Welcome To

ISSCC 2014
Session 30
Technologies for Next-Generation Systems

Session 30.1

8b Thin-Film Microprocessor Using a Hybrid Oxide-Organic Complementary Technology with Inkjet-Printed P^{2}ROM Memory

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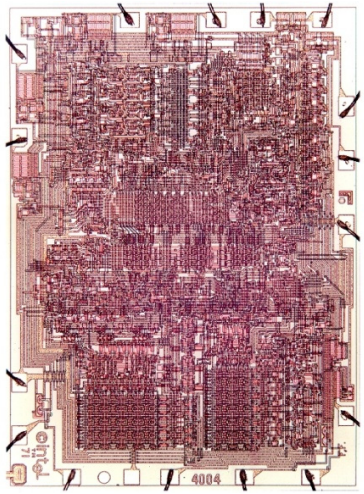
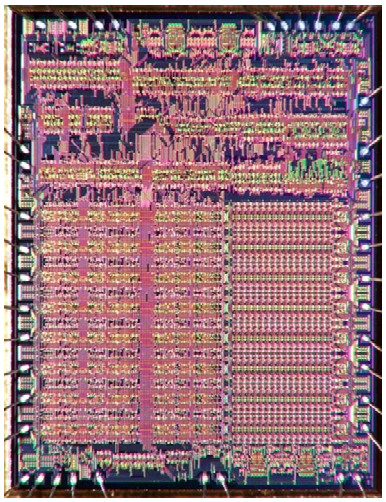
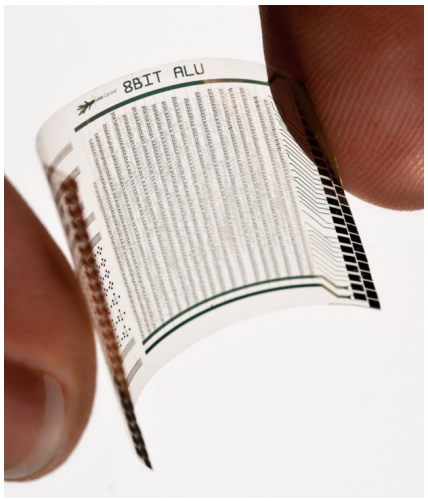
[2] KULeuven, Leuven (Belgium)
[3] Panasonic, Osaka (Japan)
[4] Evonik Industries, Marl (Germany)
[5] Holst Centre/TNO, Eindhoven (The Netherlands)

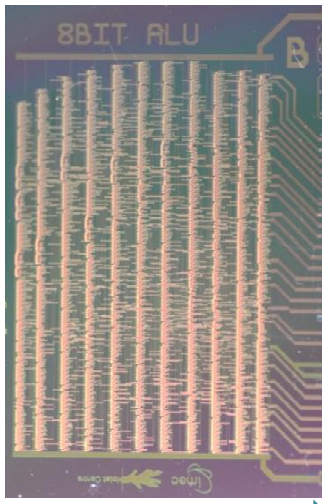
History

Intel 4004 RCA CDP1802









1971 1976 2011 2014

P-type Si
92k IPS

Si CMOS
~100k IPS

Plastic
p-type
6 (40) IPS

Plastic
p + n
2.1k IPS

Outline

- Introduction
- Technology
- Implementation
  - Processor core chip
  - P^2ROM chip
- Benchmarking
- Conclusions

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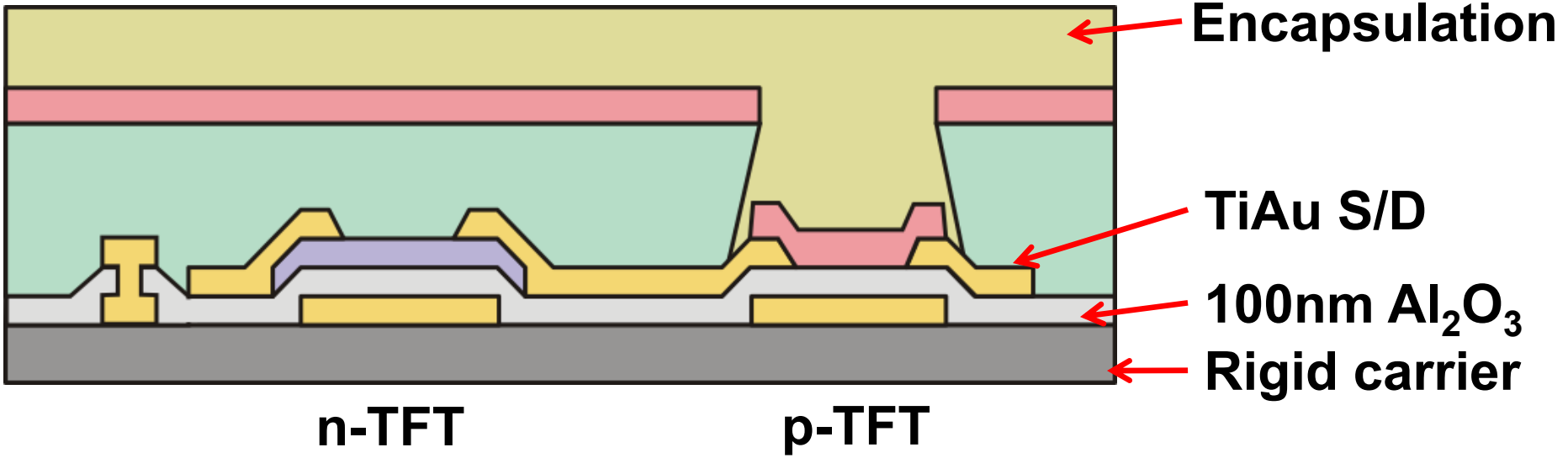
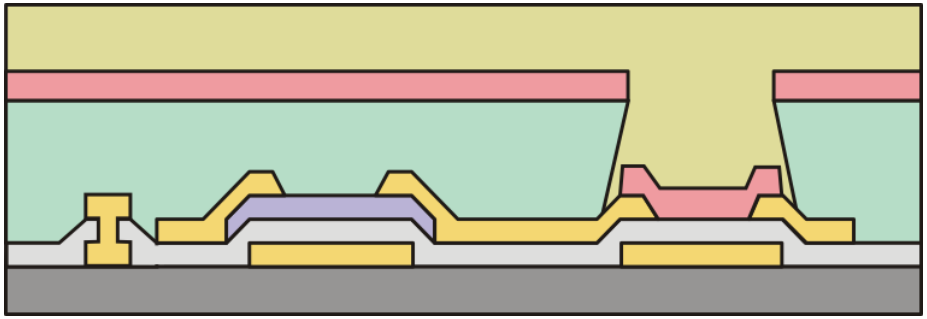
Hybrid complementary technology

- **Solution-processed metal-oxide (n-TFT)**
- **Evaporated organic (p-TFT)**

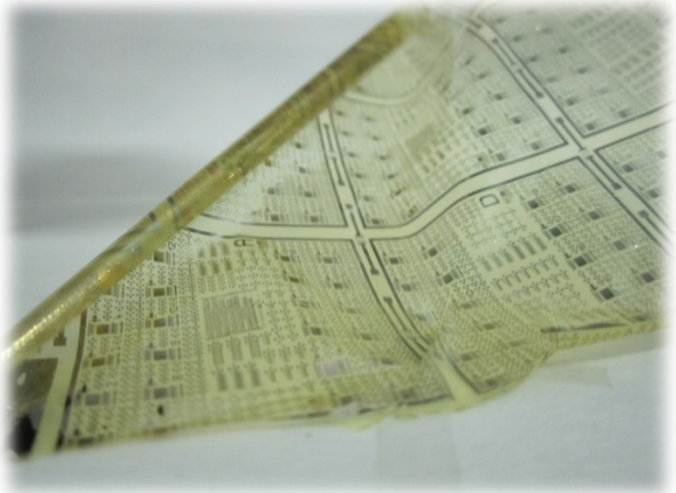


Hybrid complementary technology



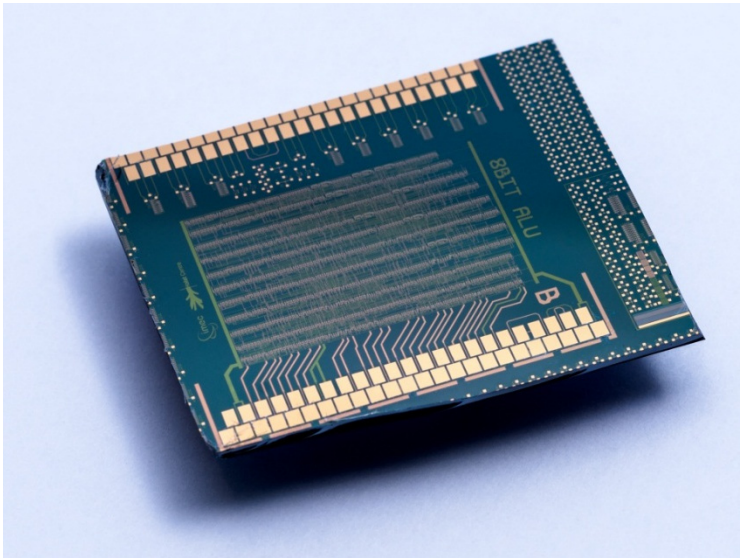
Process temperature ≤ 250C

➔ enabling foil integration



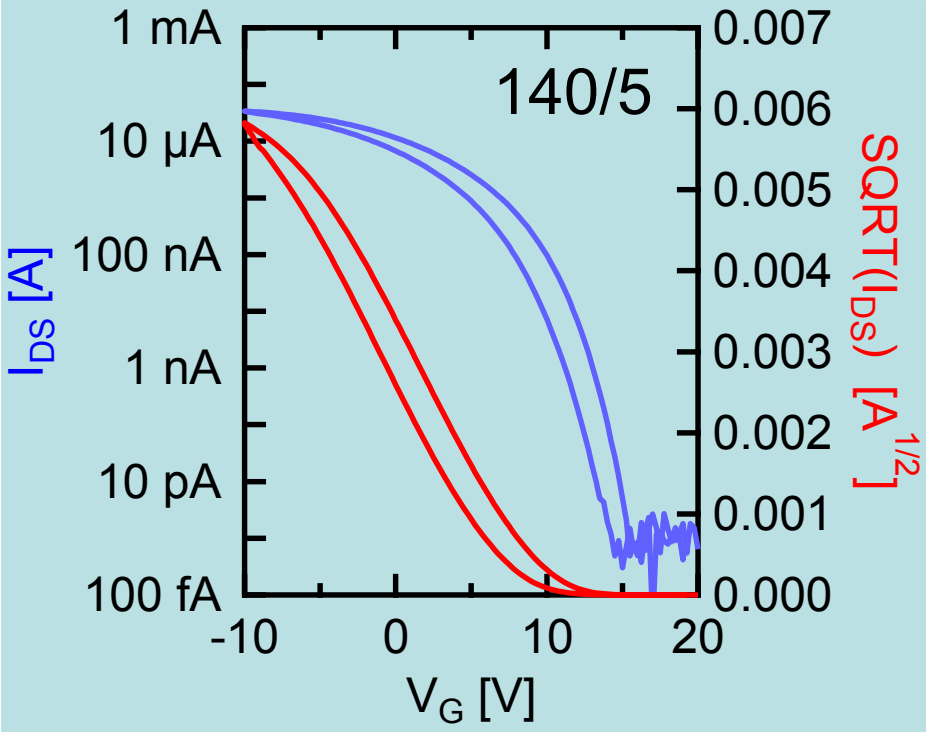
M. Rockelé, IDW 2011

Here: rigid substrate



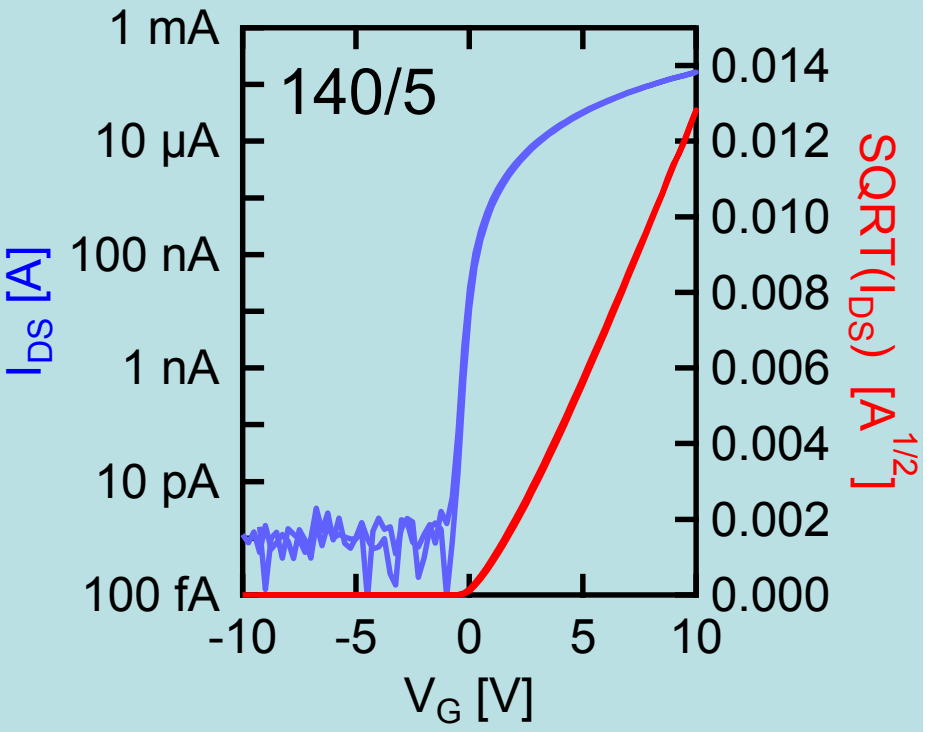
Hybrid complementary technology

Organic p-TFT



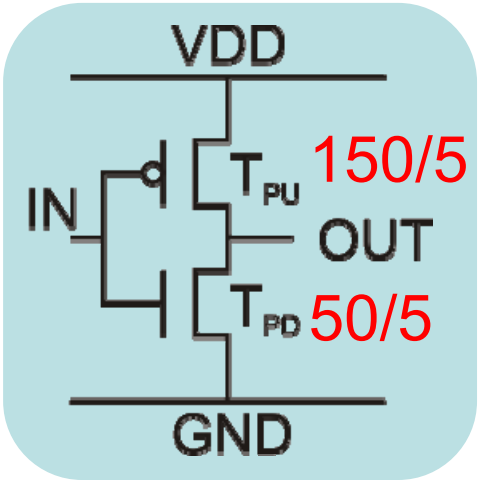
µ ~ 0.14 cm²/Vs

Metal-oxide n-TFT



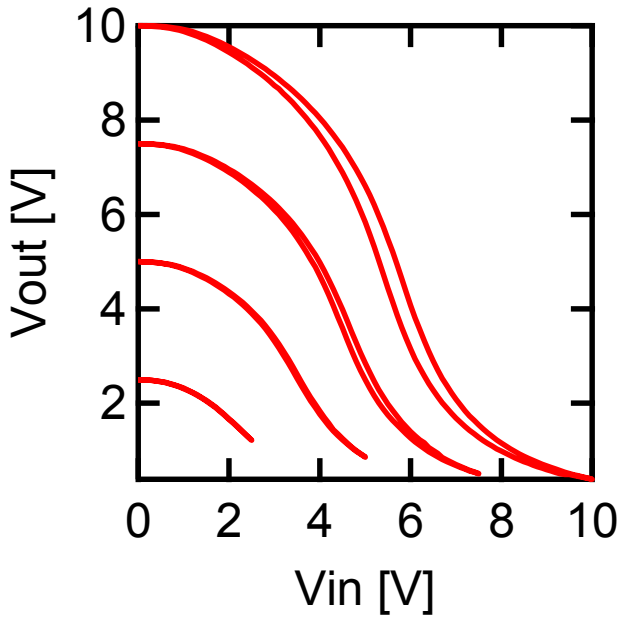
µ ~ 2 cm²/Vs

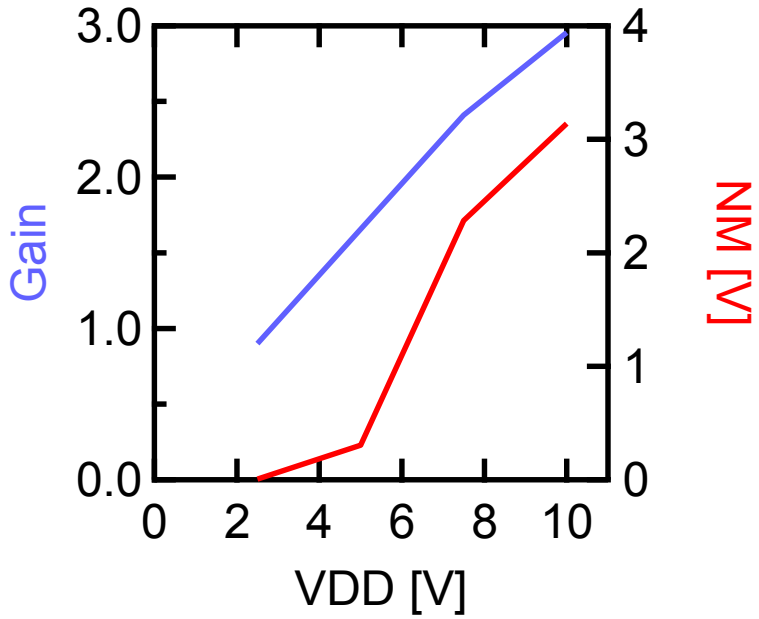
Hybrid complementary technology



p:n ratio ~ 3:1 for matching

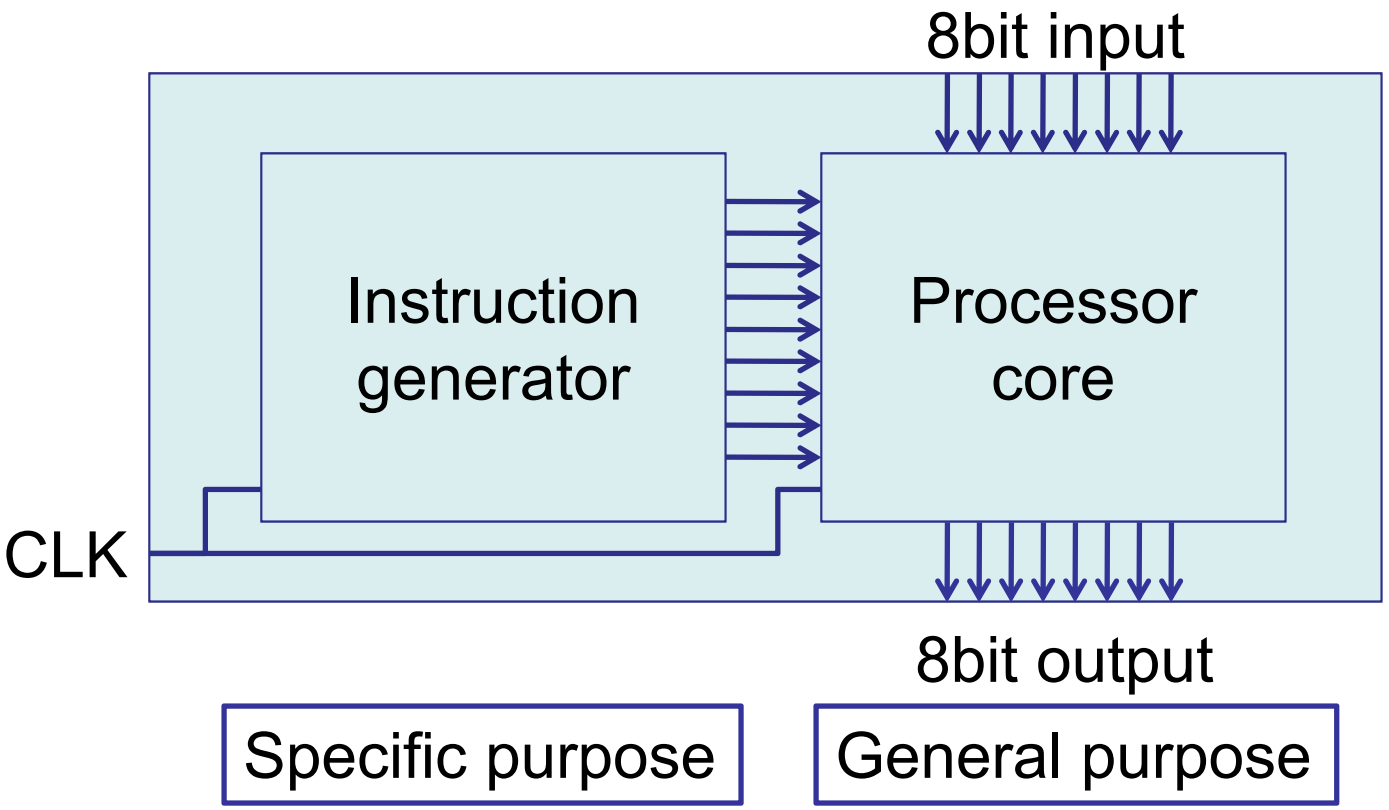
- **μ (p) < μ (n)**
- **p-TFT depletion device**





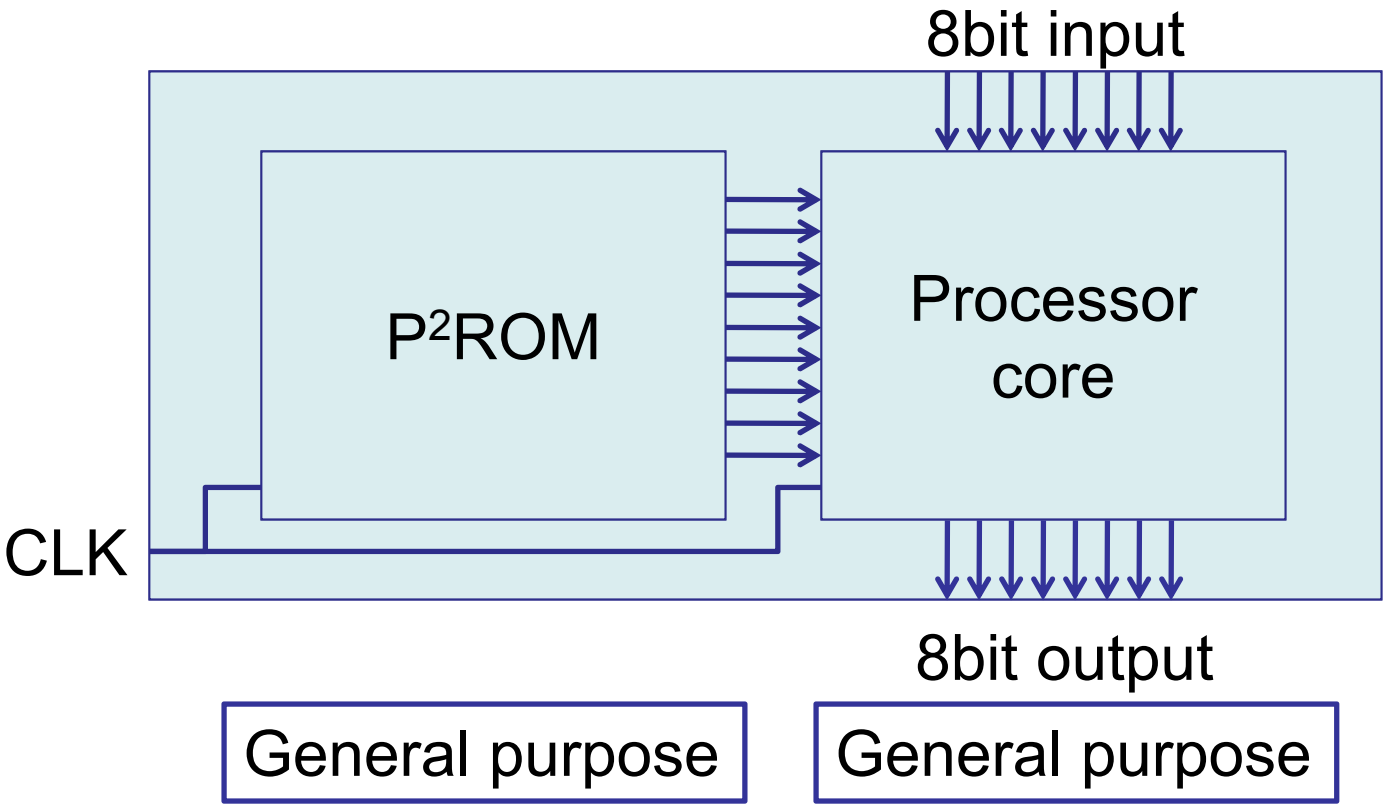
Status ISSCC 2011

- Complete microprocessor integrated on foil:
  - Processor core foil
  - Instruction generator foil (hard-coded ROM)



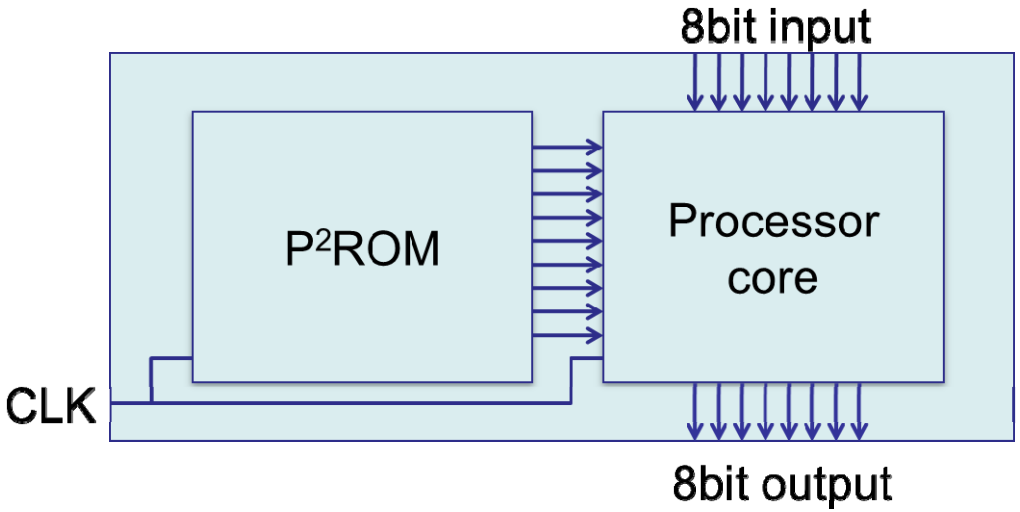
2011 → 2014: Configurable design

- Complete microprocessor integrated:
  - Processor core-chip
  - P²ROM instruction generator



Outline

- Introduction
- Technology
- Implementation
  - Processor core chip
  - P²ROM chip
- Benchmarking
- Conclusions



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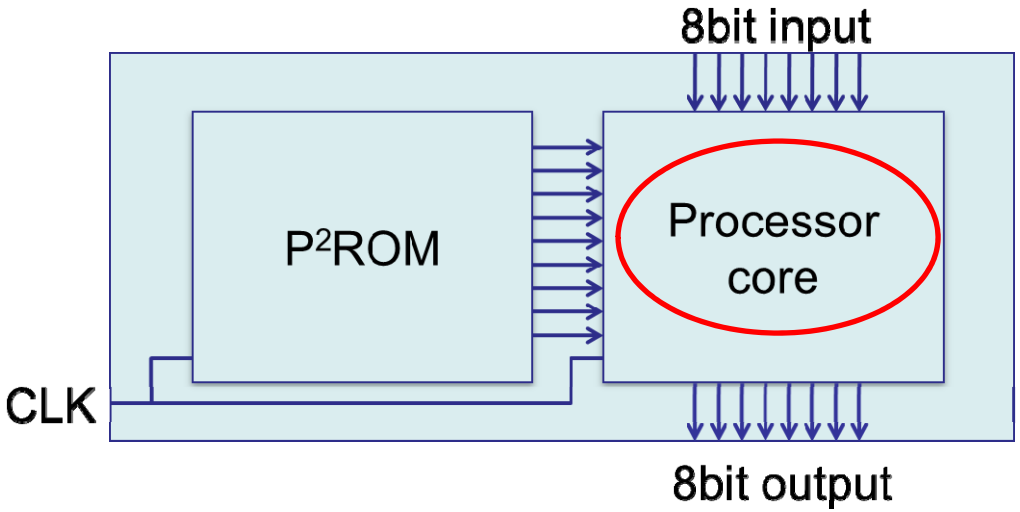


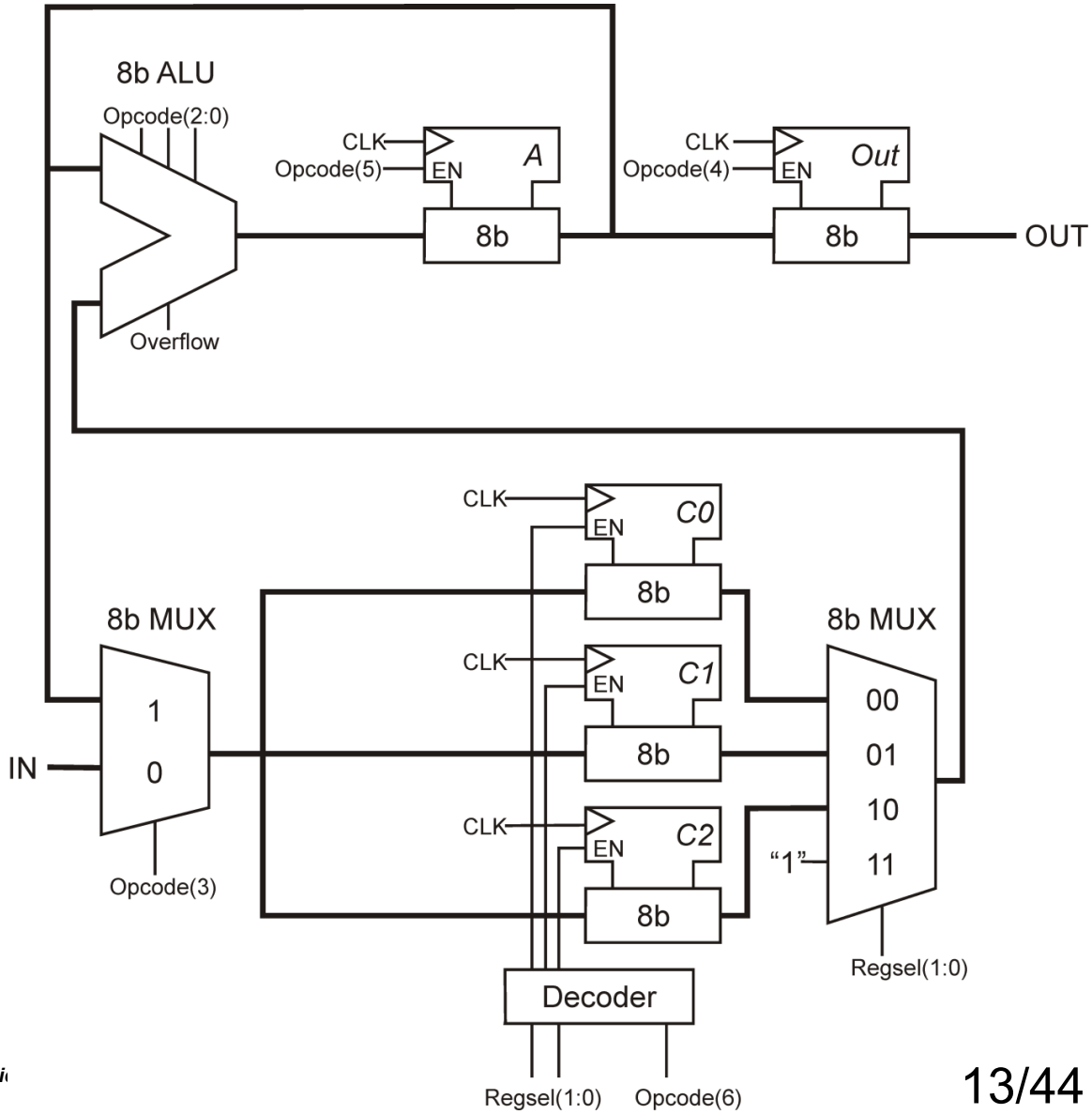
General purpose processor core

8b processor core

- Arithmetic
- Logic
- Bit shifting
- 8b Registers

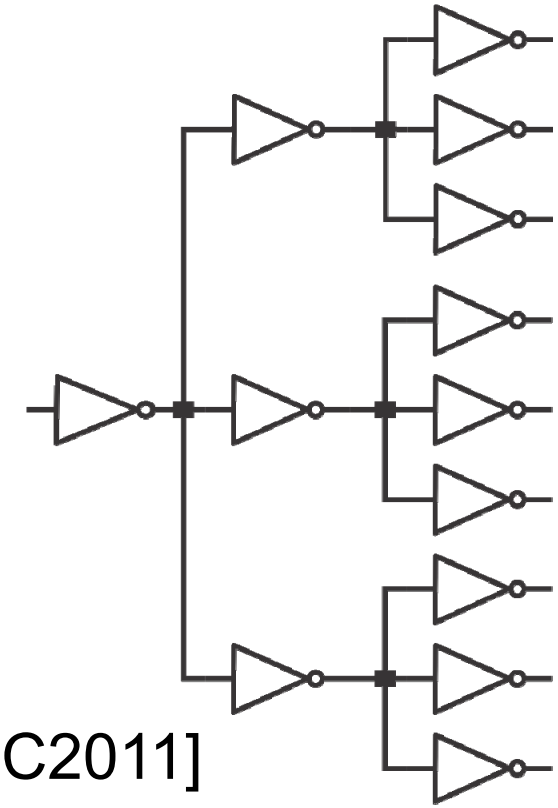
Improvements

- Signal buffering
- Mirror adder
- Extended library



Improved signal buffering

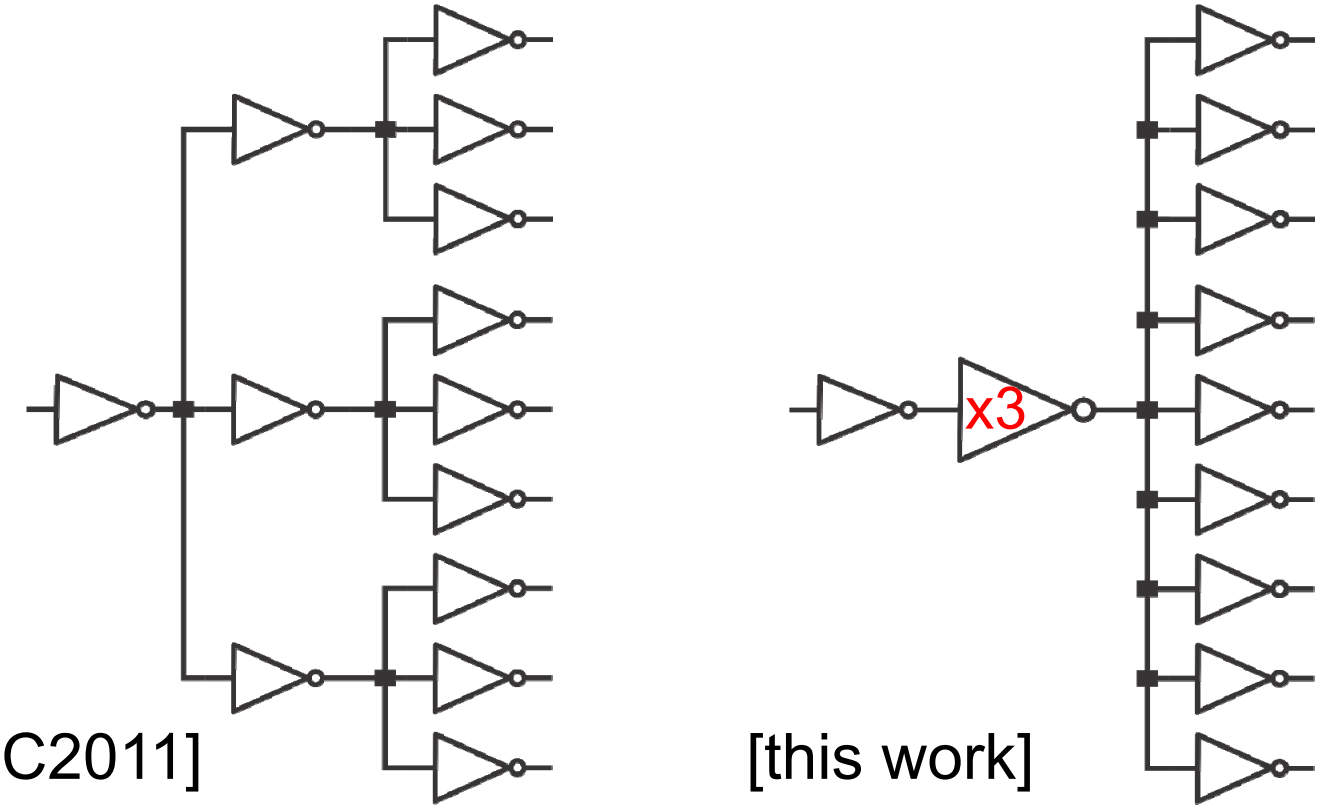
- Tree-like implementation [ISSCC2011]
  - Due to limited library



[ISSCC2011]

Improved signal buffering

- Tree-like implementation [ISSCC2011]
  - Due to limited library
- Dedicated buffers reduce gate count [this work]



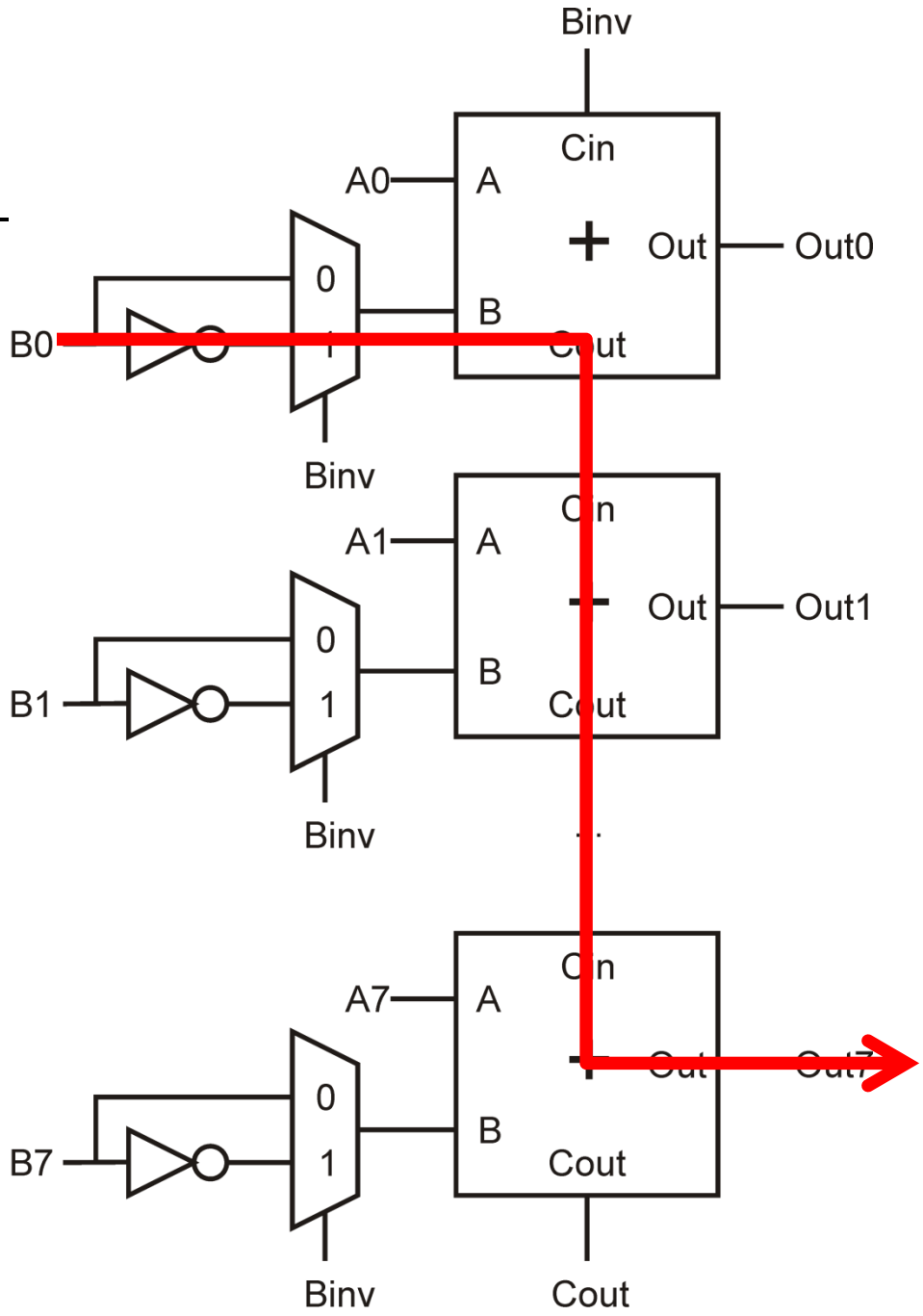
[ISSCC2011] [this work]

Arithmetic unit

- ADD
- SUB
- INC
- DEC

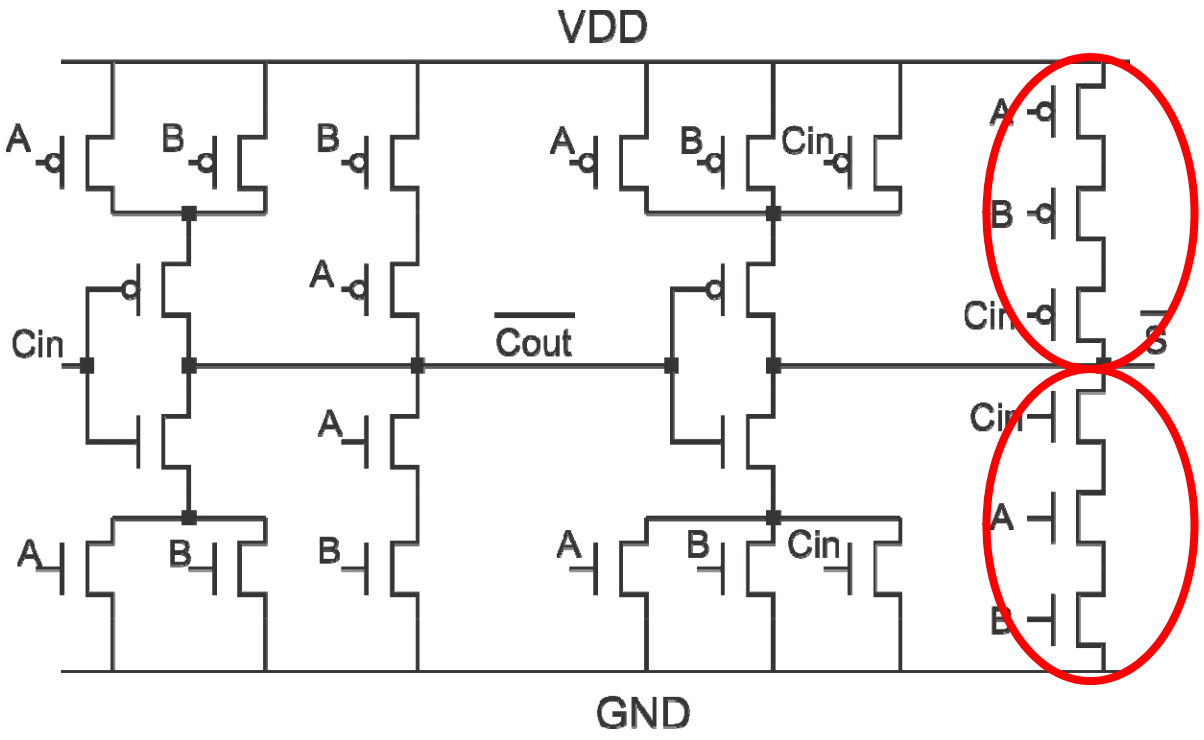
Ripple carry adder/subtract

Long critical path



Mirror adder cell

- Mirror adder integrated in 8b ripple carry adder
- Adapt 8b adder for inverted outputs



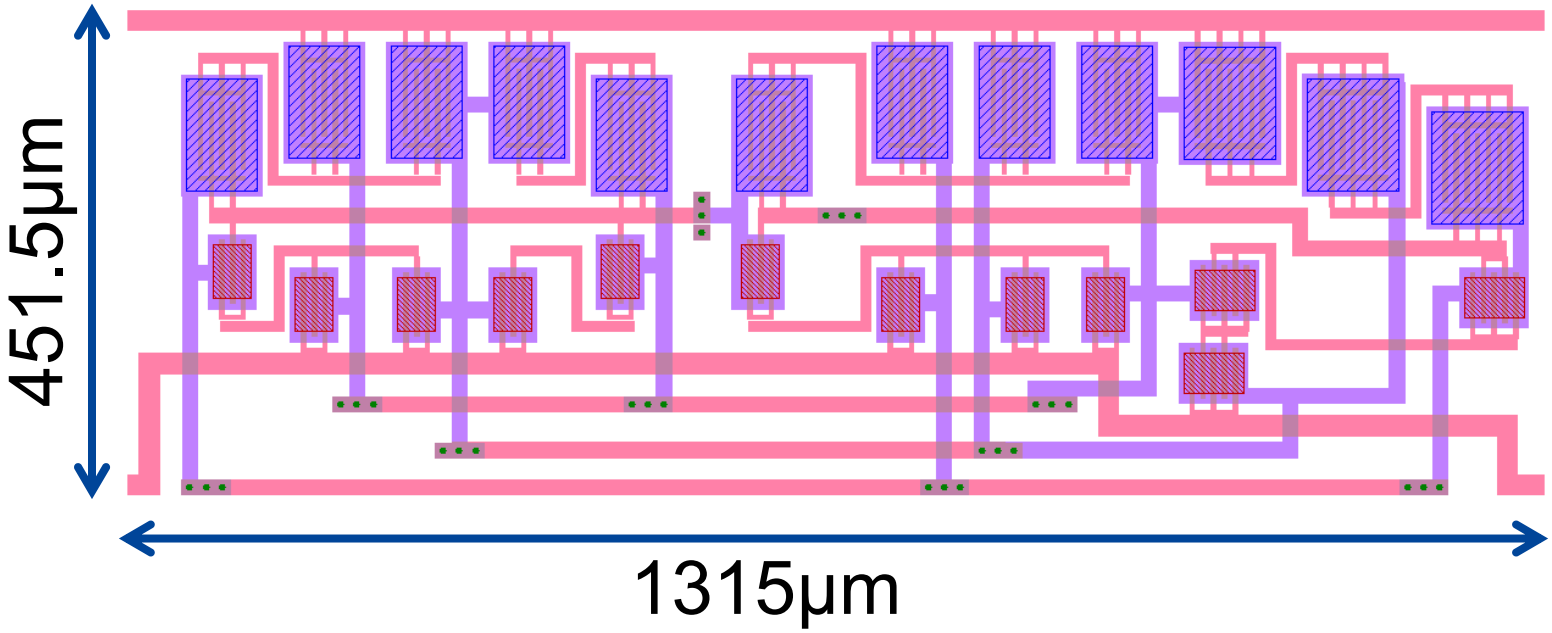
+ less TFTs
+ faster adder

- NOR3-like structure

Rabaey *et al.*, Prentice Hall

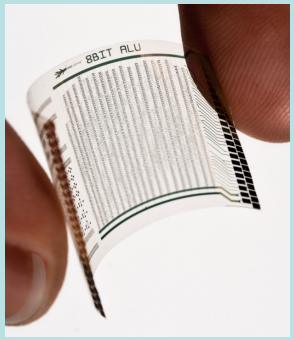
Mirror adder cell layout

- Mirror adder integrated in 8b ripple carry adder
- Adapt 8b adder for inverted outputs



Extended standard cell library

2011



Core

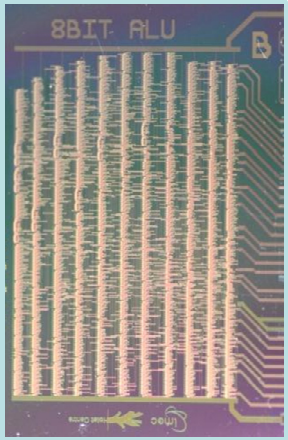
- INV
- NAND2

Output buffer

- INV3

p-type only

2014



Core

- INV
- INV3
- INV4
- INV9
- NAND2
- NAND2_BUF2
- FA_mirror

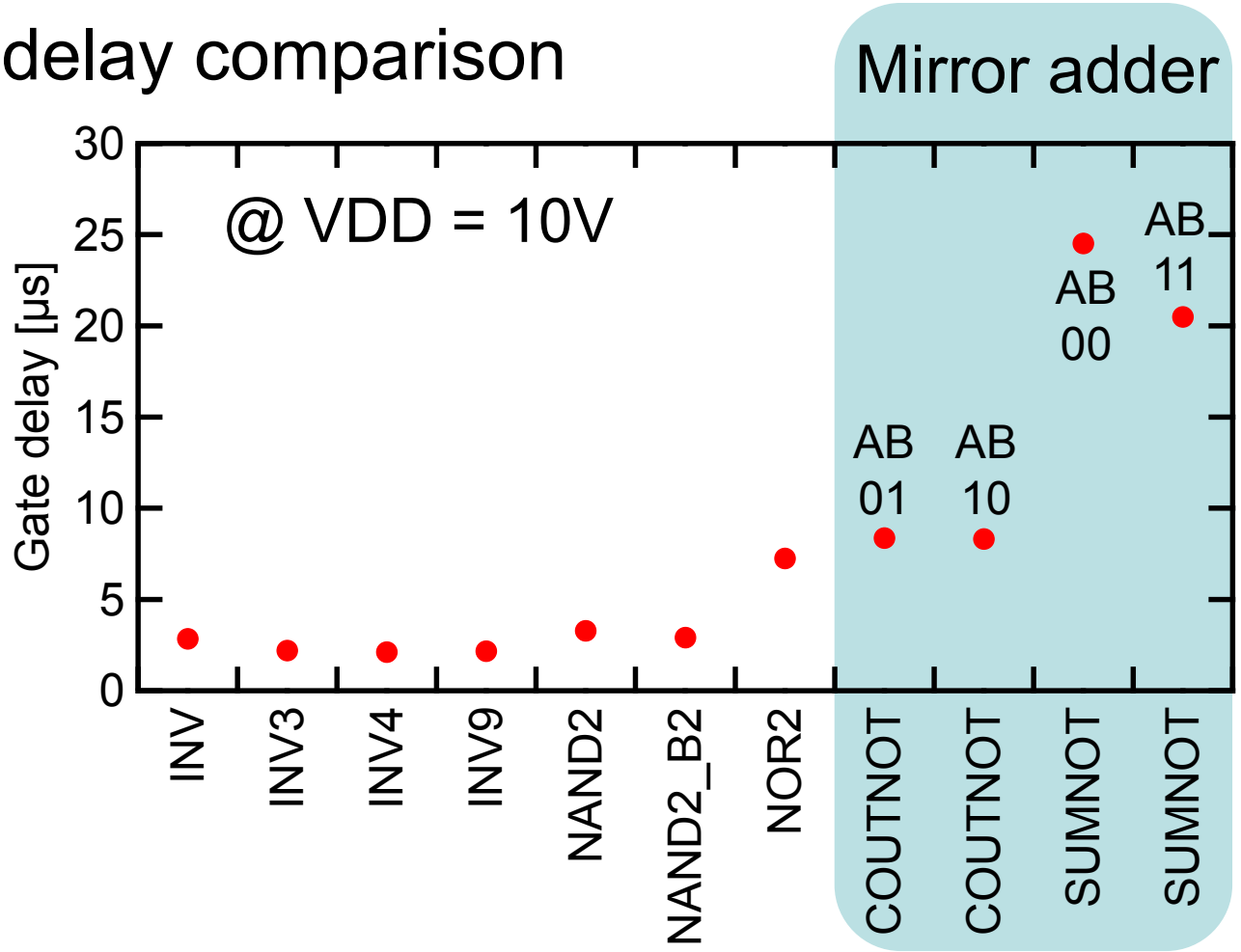
Output buffer

- INV4

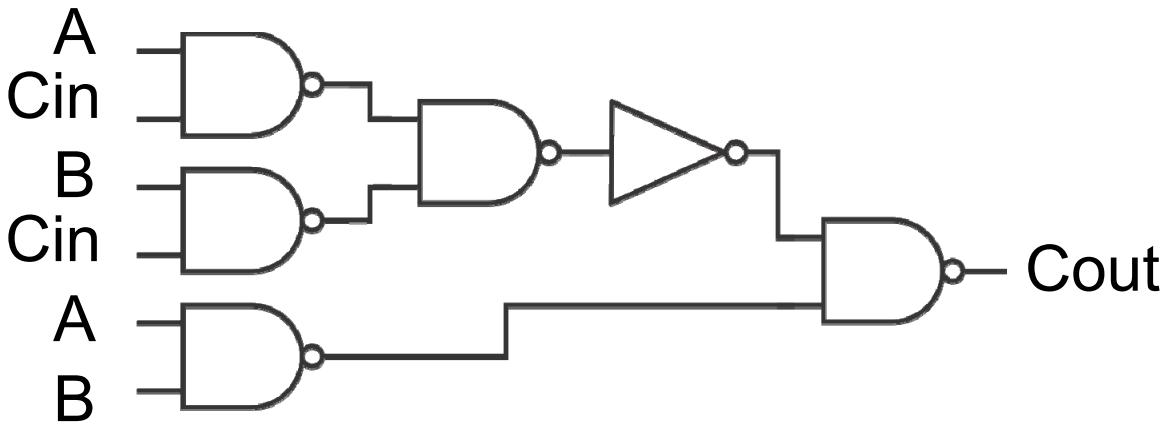
p+n

Standard cell delays

- All cells integrated in 19-stage ring oscillators
- FA delay comparison

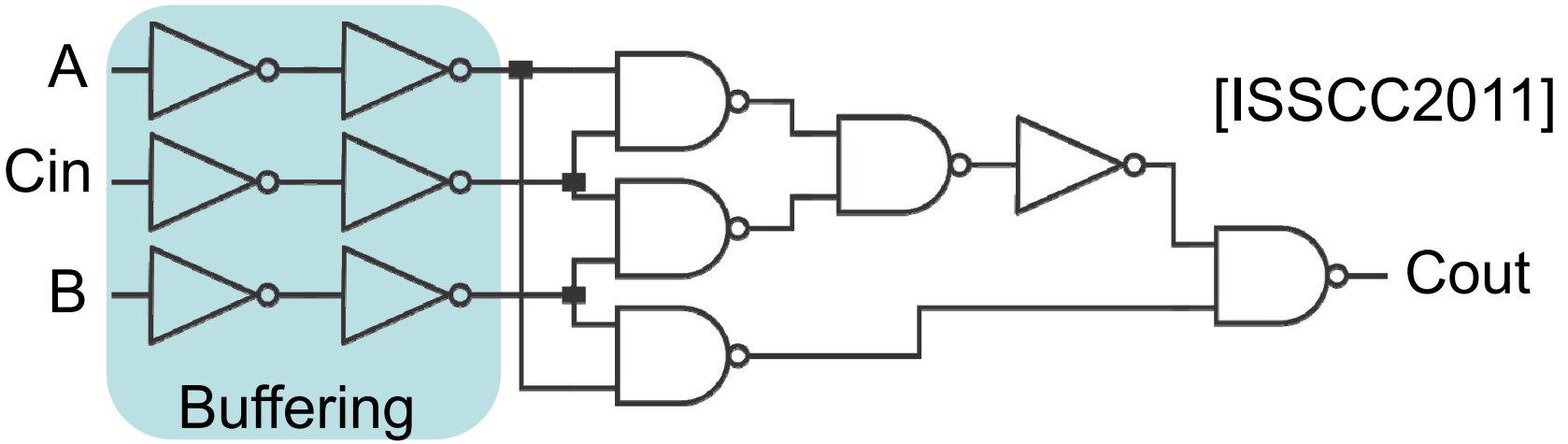


Full adder delay: Cin → Cout



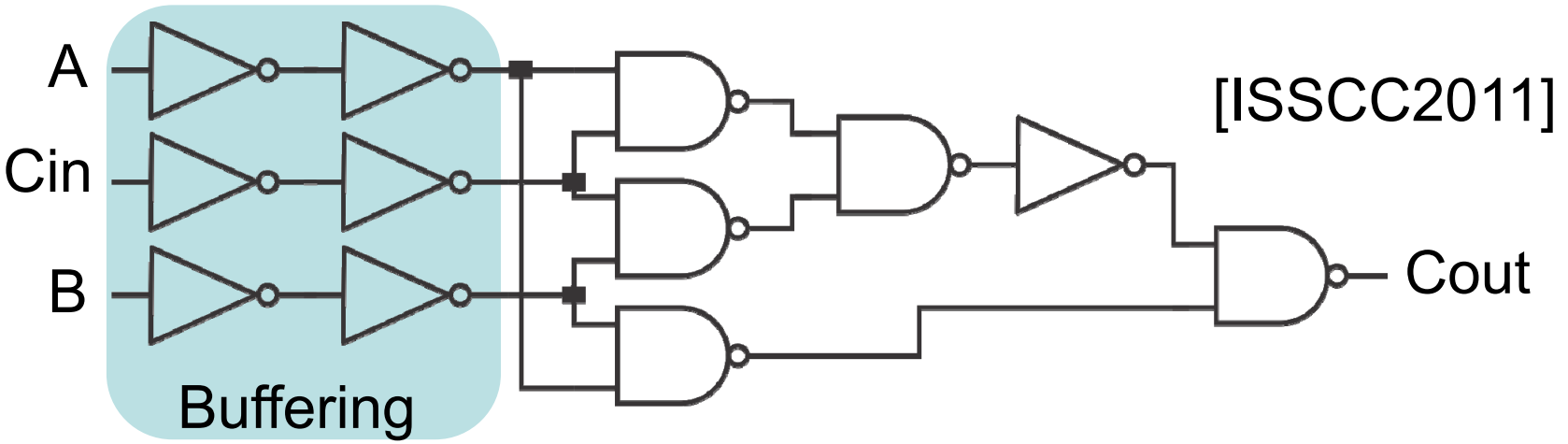
Total delay: 1 INV + 3 NAND2

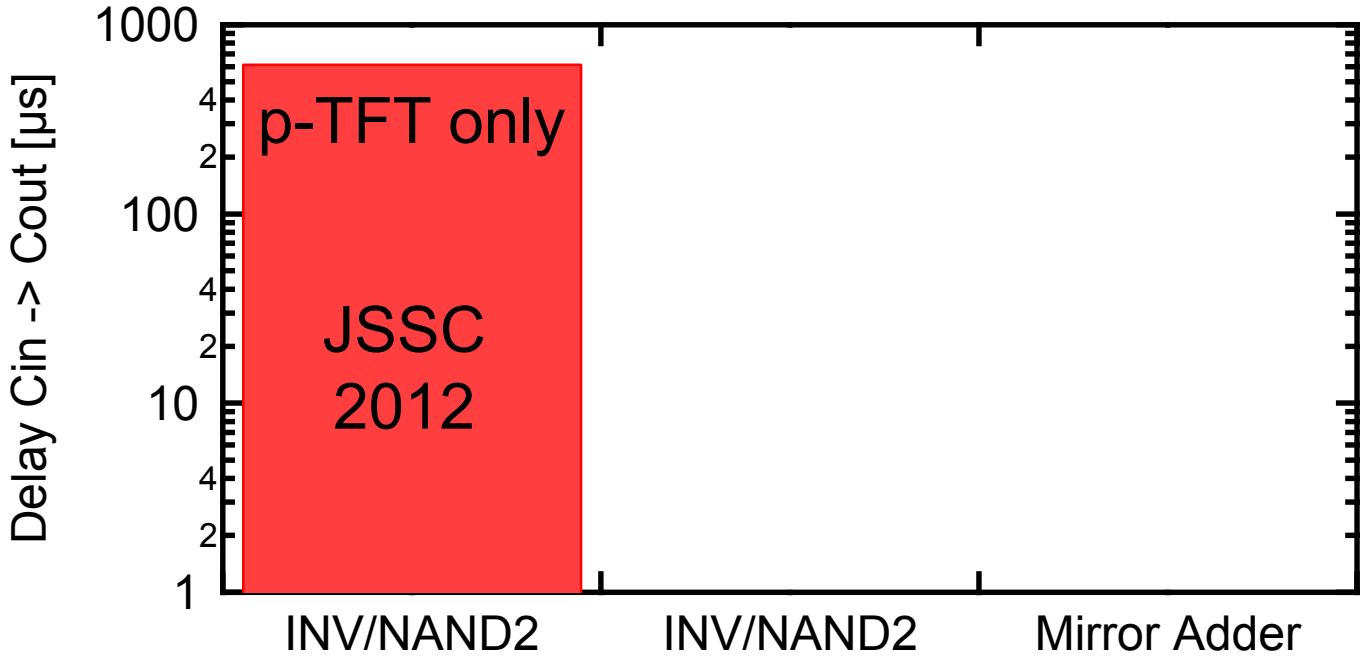
Full adder delay: Cin → Cout



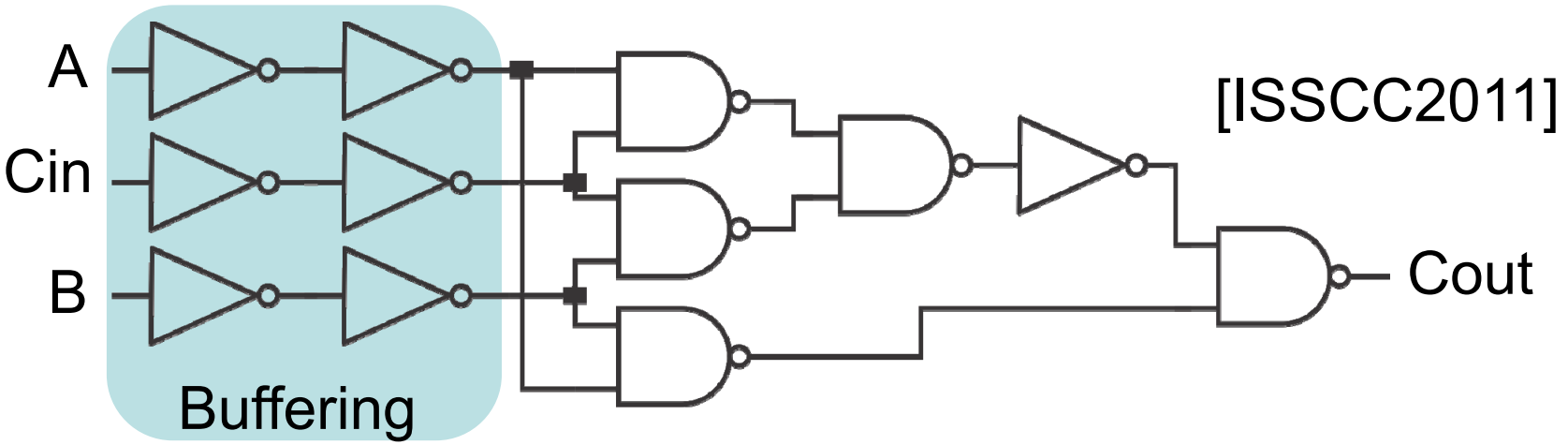
Total delay: 3 INV + 3 NAND2

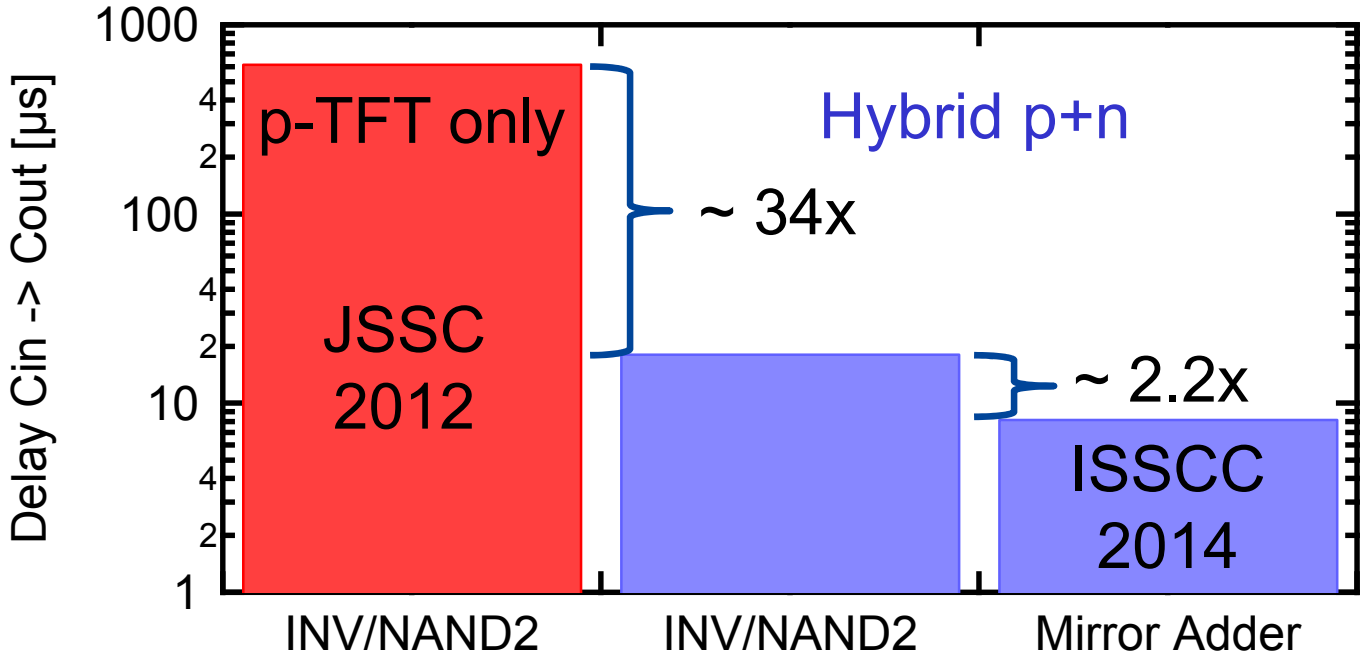
Delay characterization: Cin → Cout





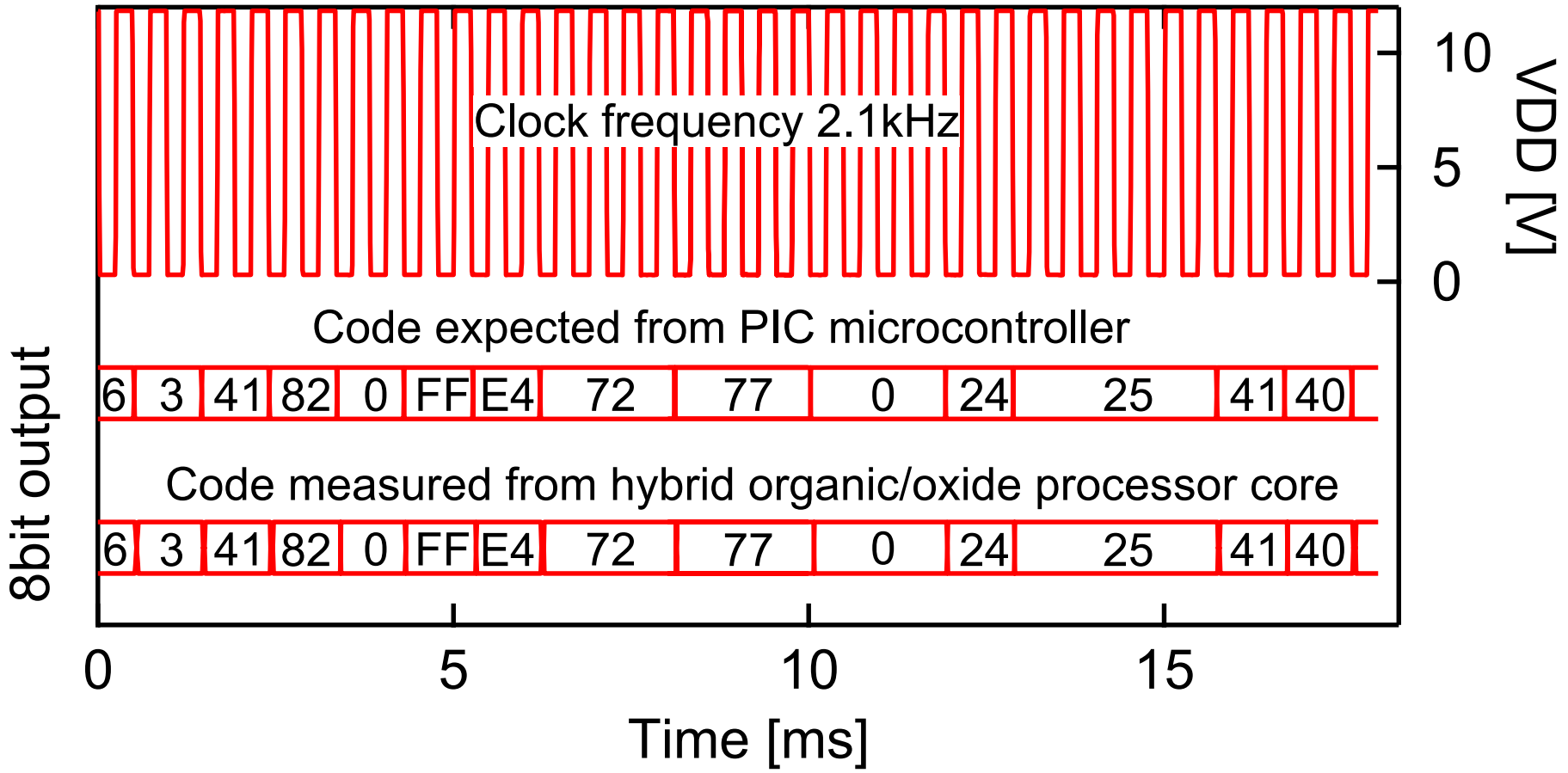
Delay characterization: Cin → Cout





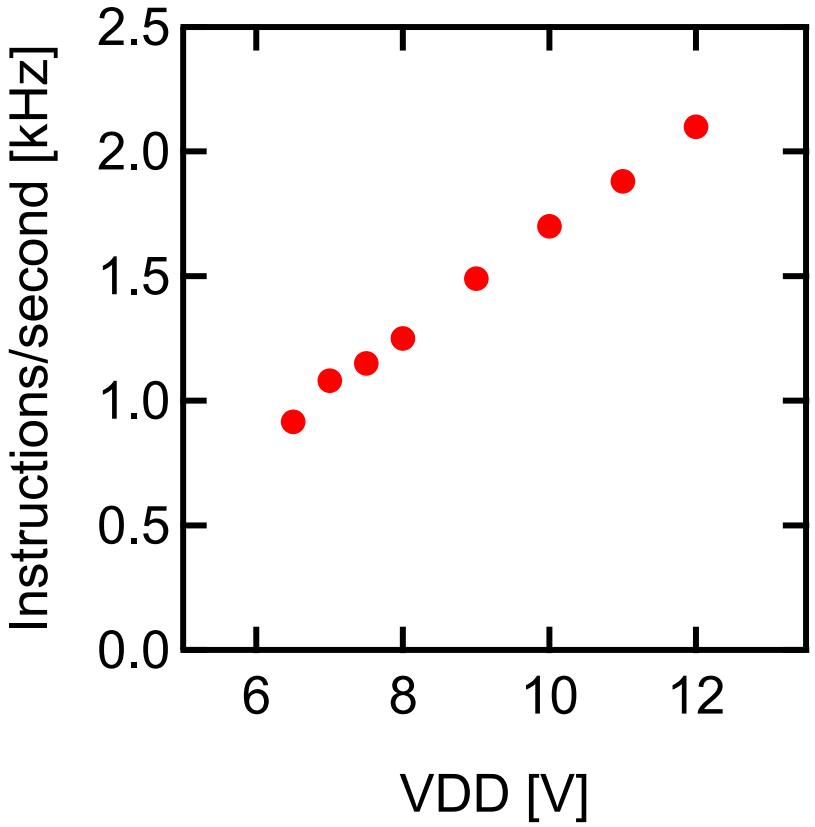
General testbench measurements

- Test all individual instructions
- Compare measured to expected output



Operation regimes

- OPS increases with VDD
- 6.5V minimal supply voltage



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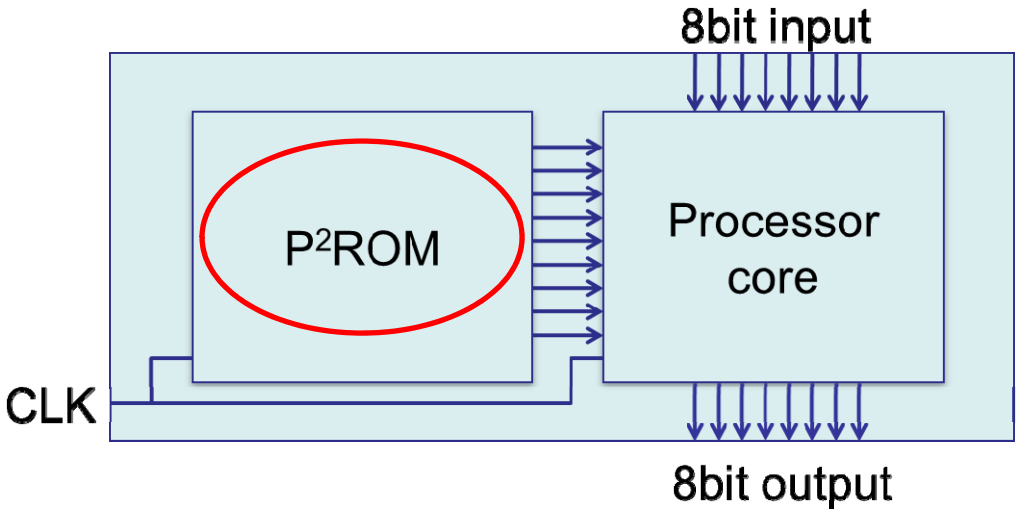
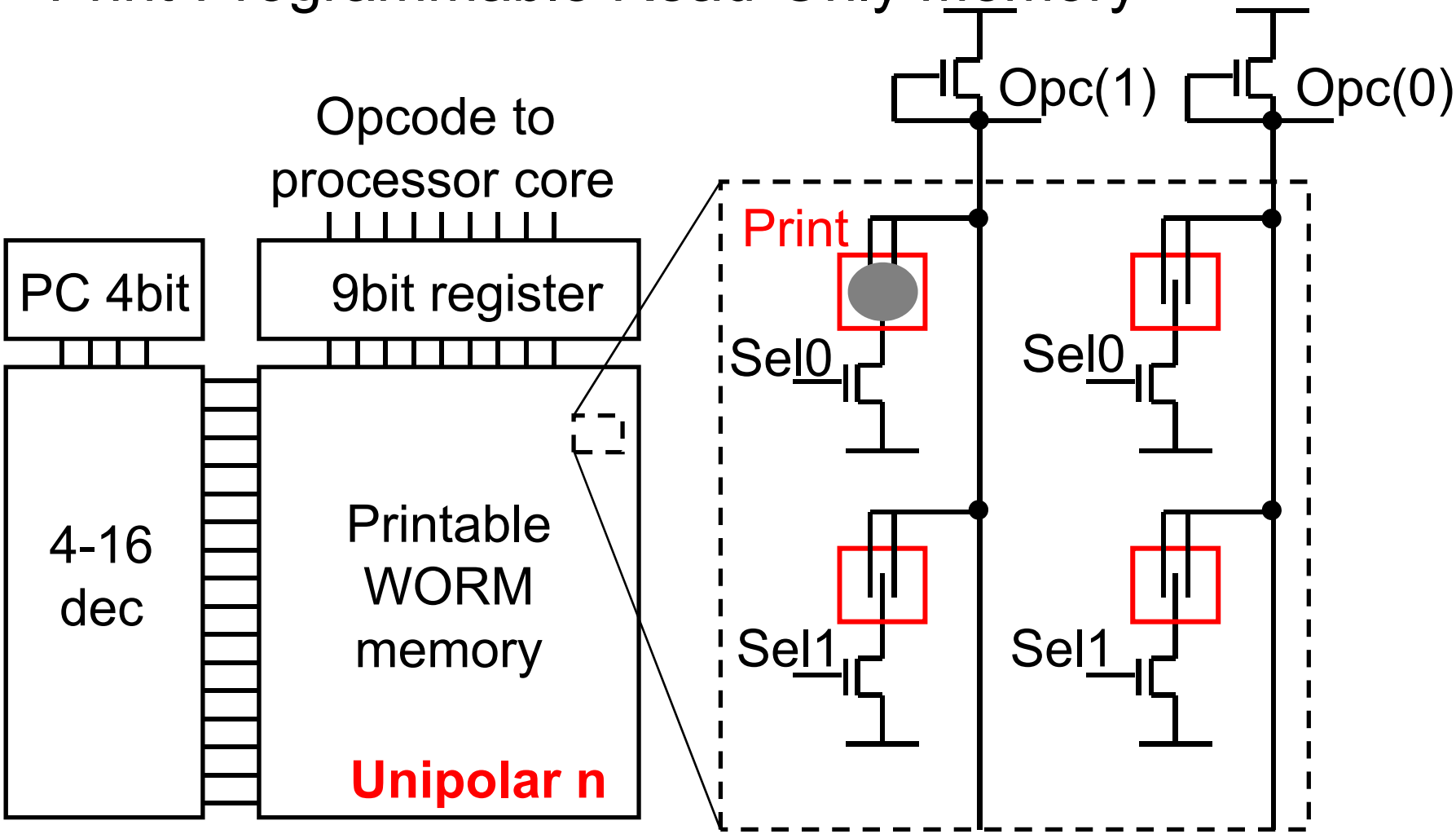
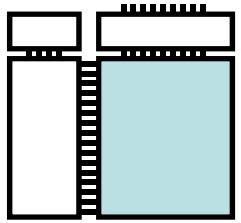


P²ROM chip

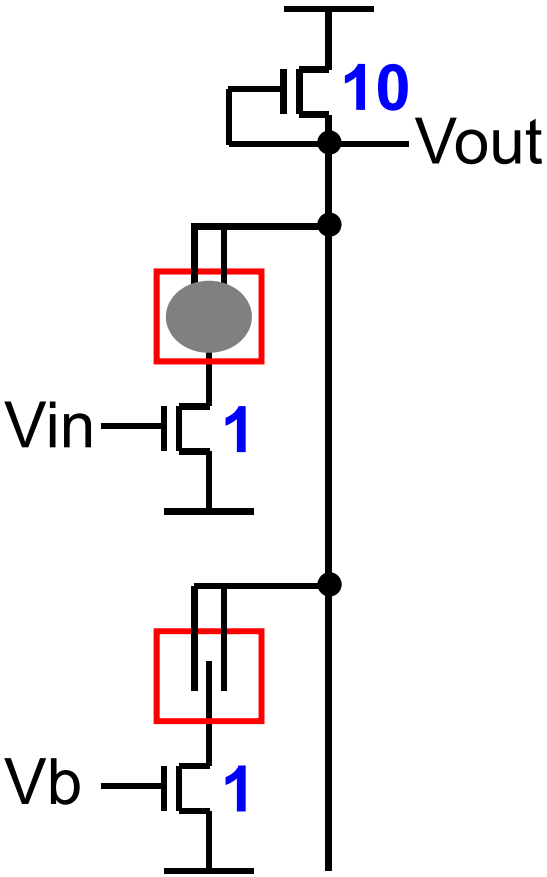
- Print-Programmable Read-Only Memory

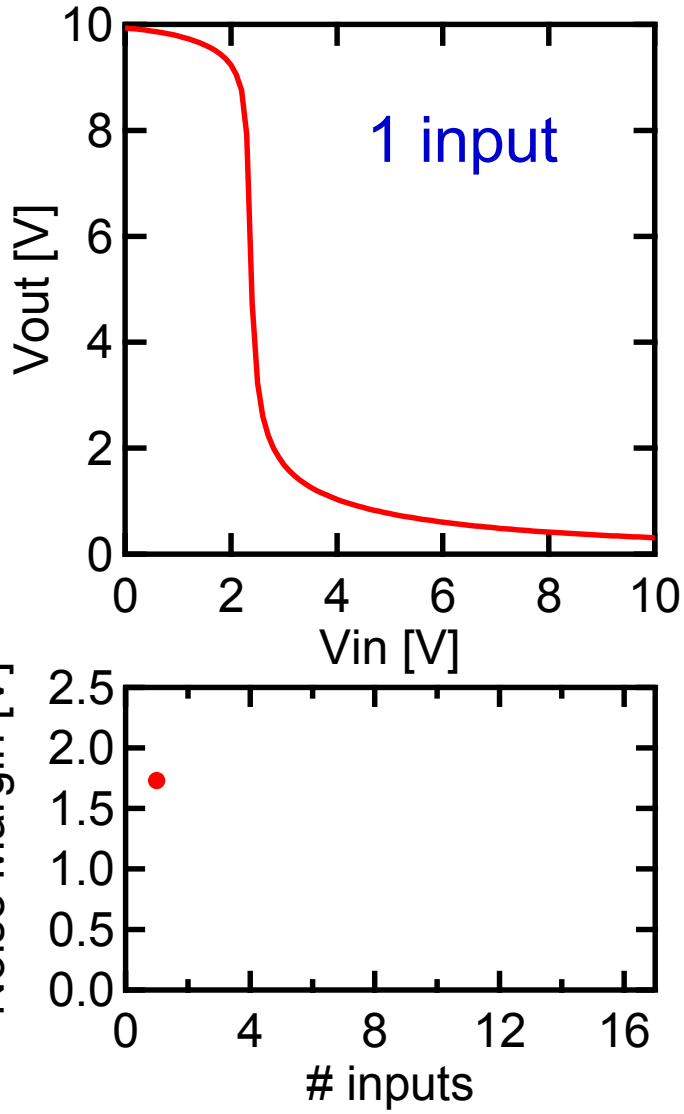


Printable WORM memory



- Unipolar depletion-load NOR
- Configurable up to 16 inputs





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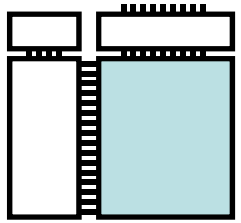

- Unipolar depletion-load NOR
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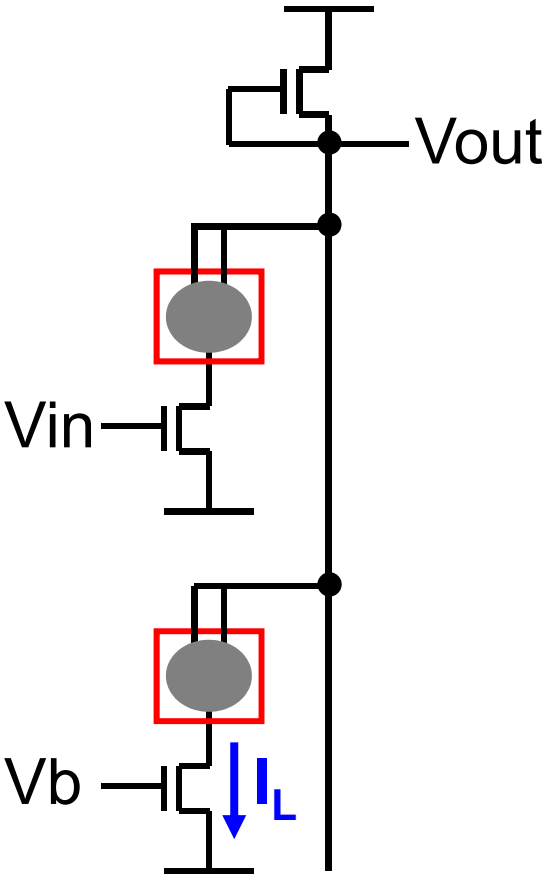
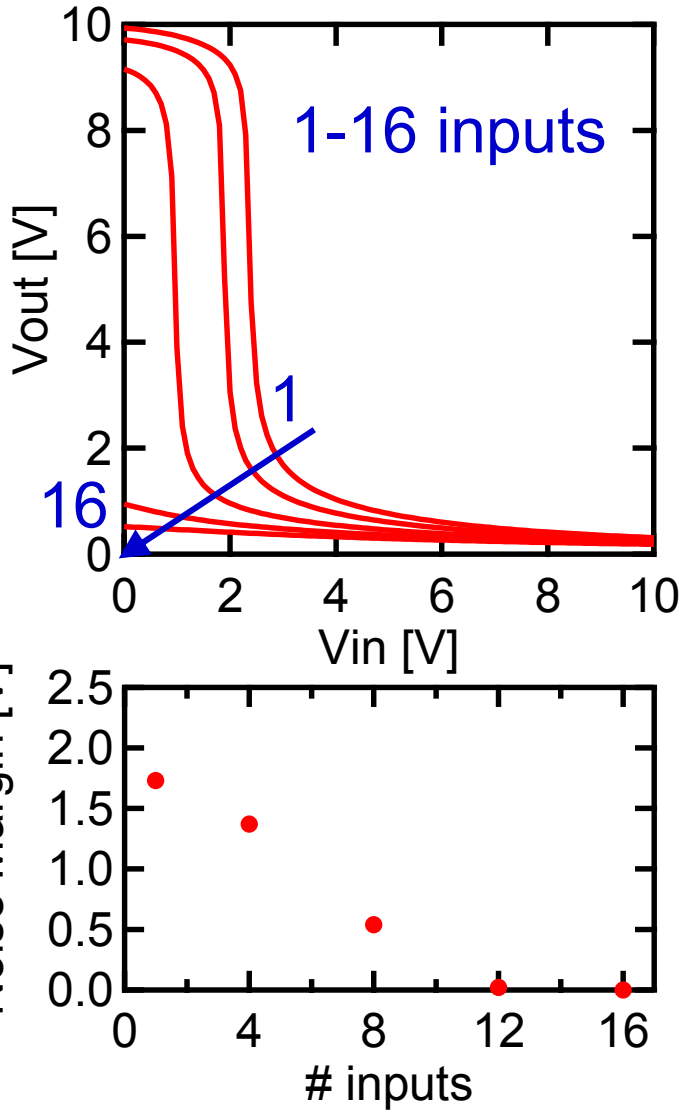
Robustness issue





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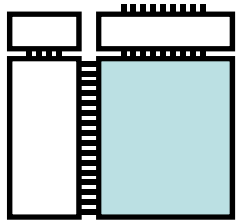

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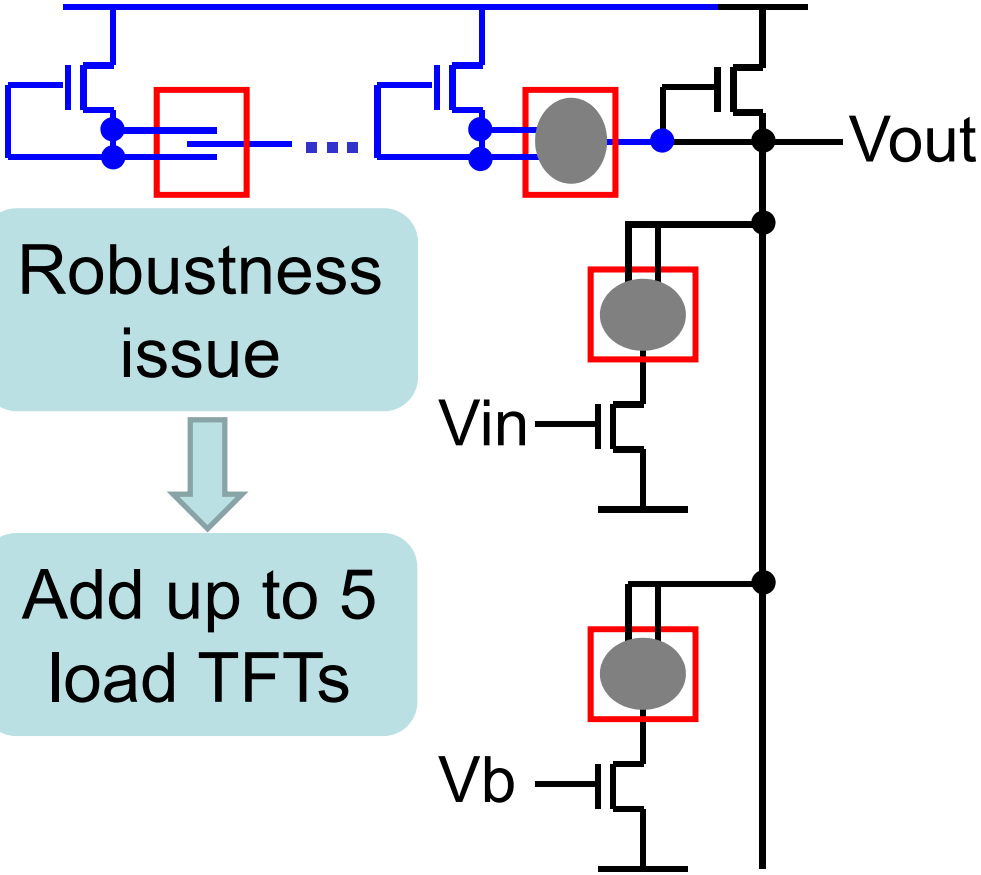
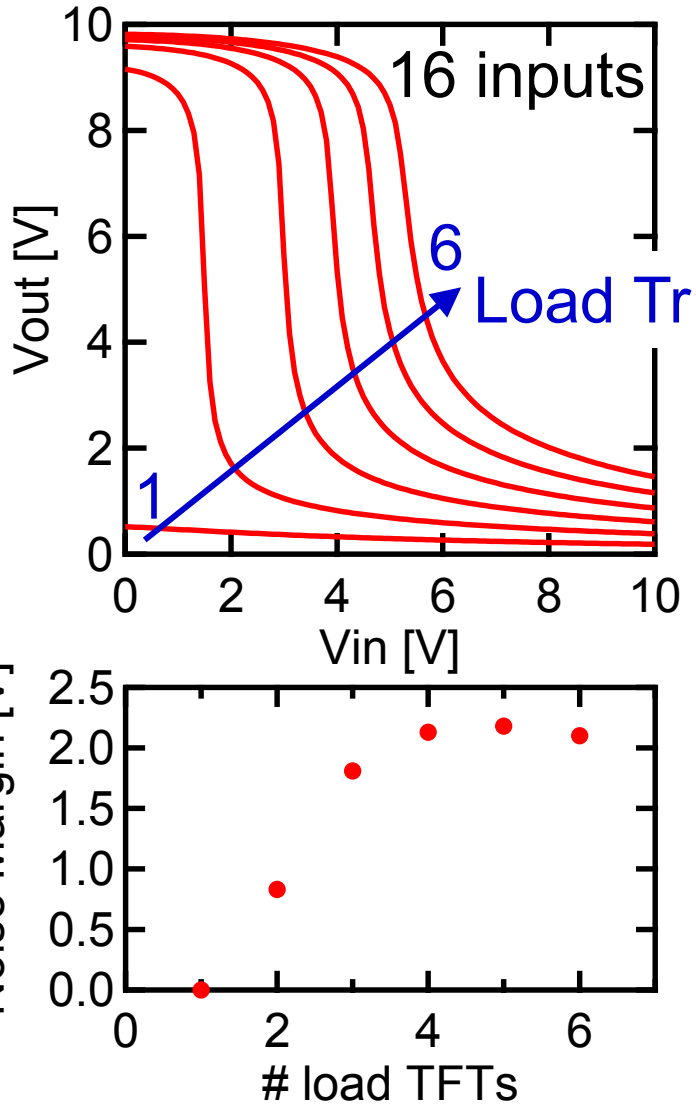
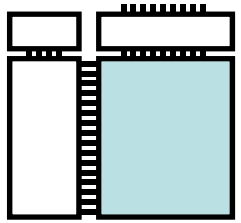


Robustness issue

Add up to 5 load TFTs

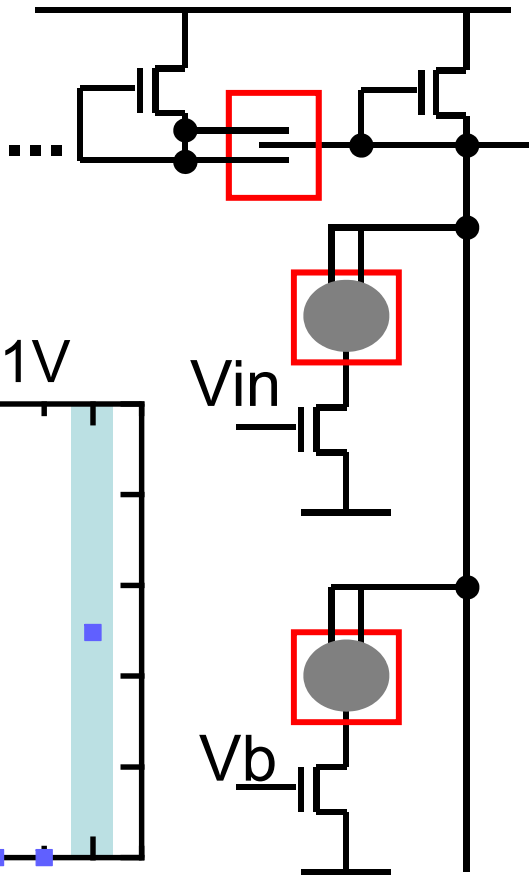


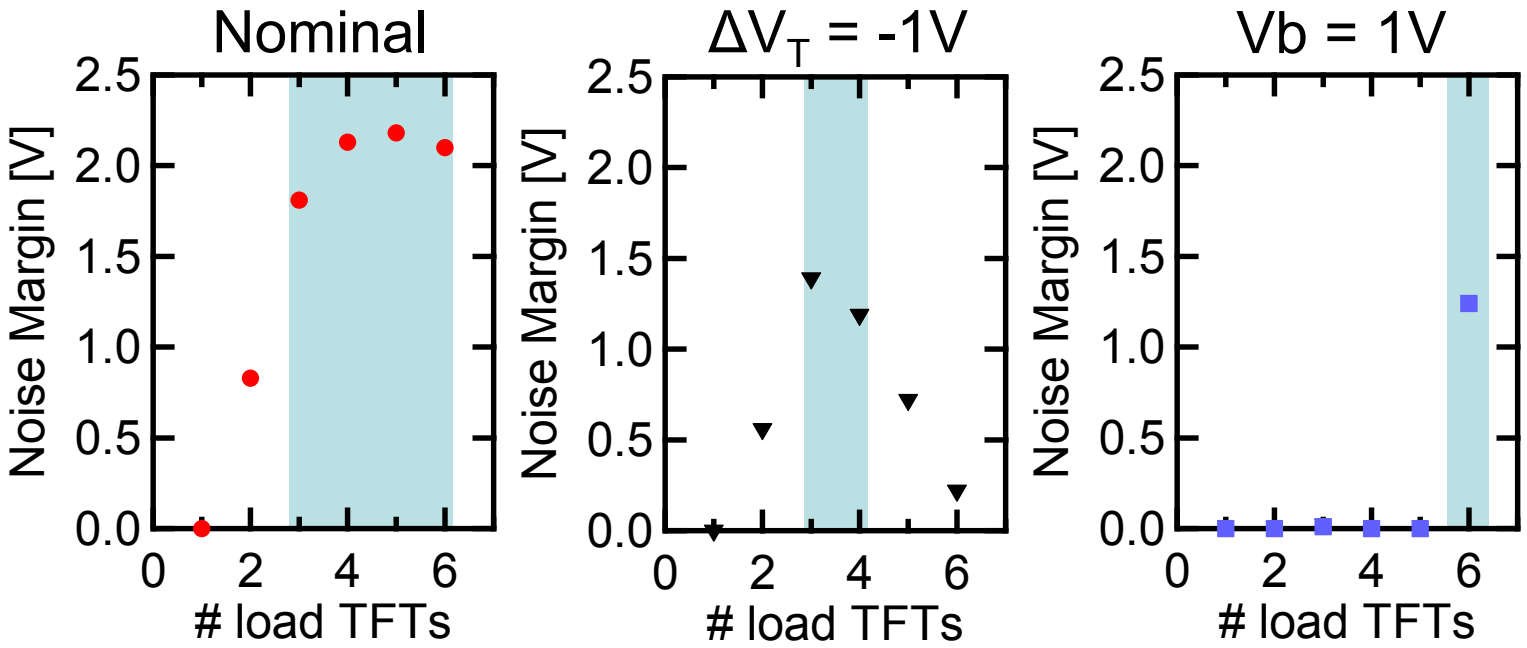
Printable WORM memory



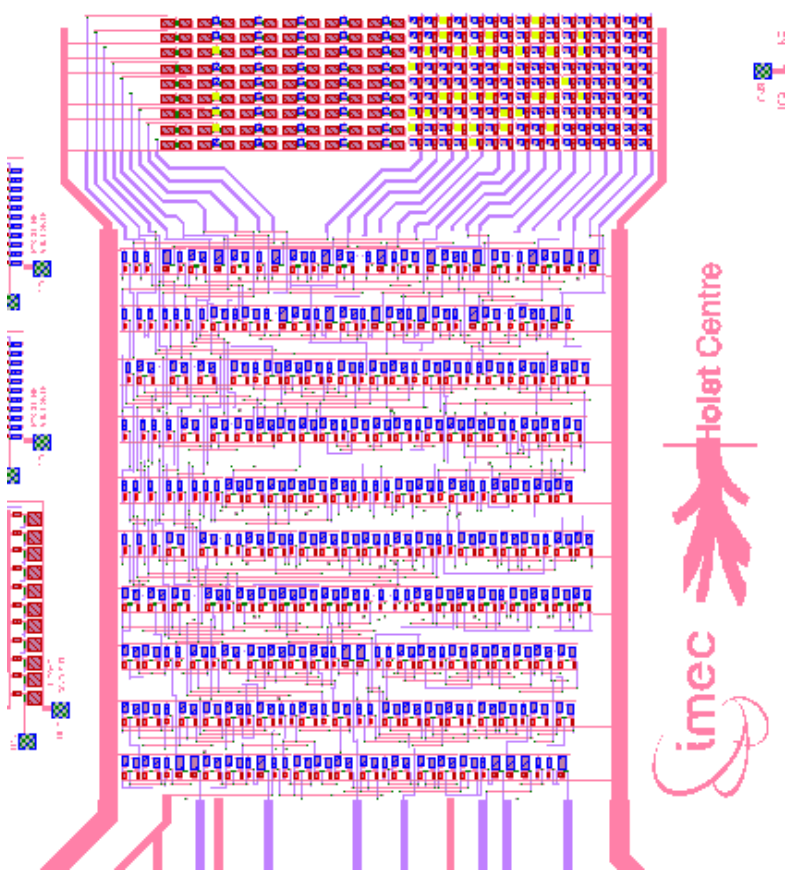
- Post-fabrication compensation technique for
  - Number of drive TFTs
  - Process corners, variability
  - Gate voltage variations at Vb

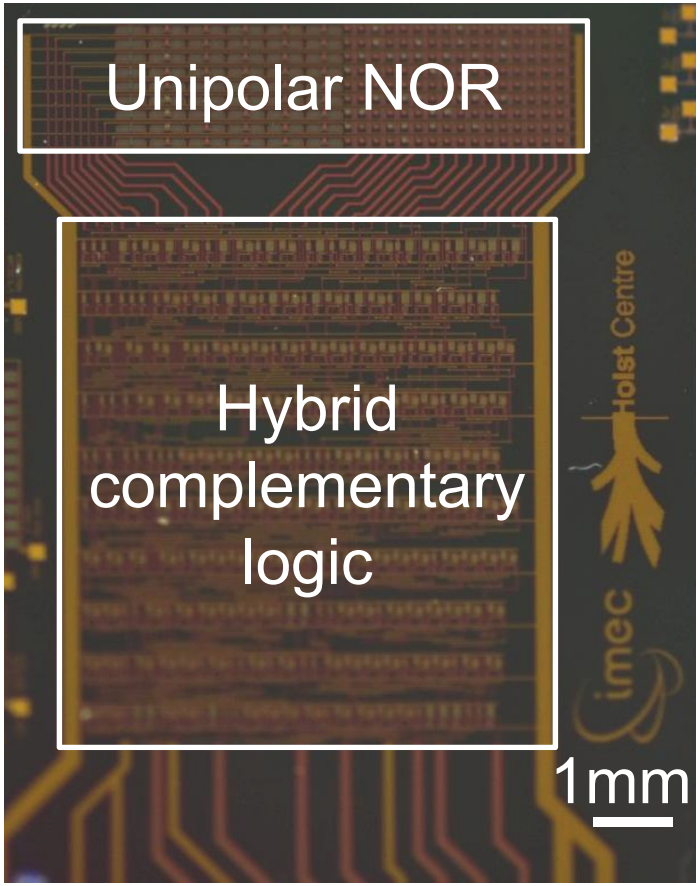
16 input NOR



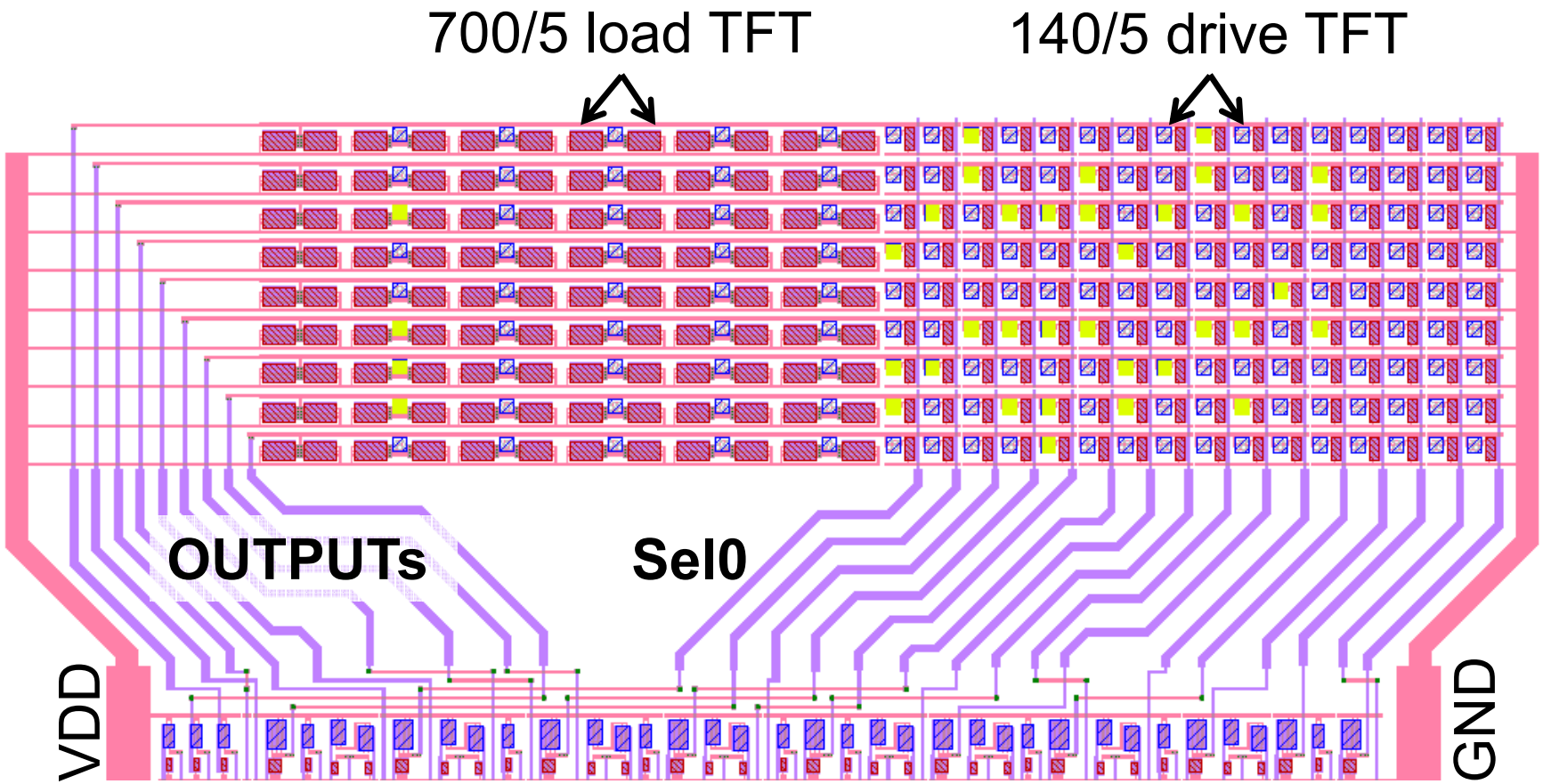


Layout P²ROM chip

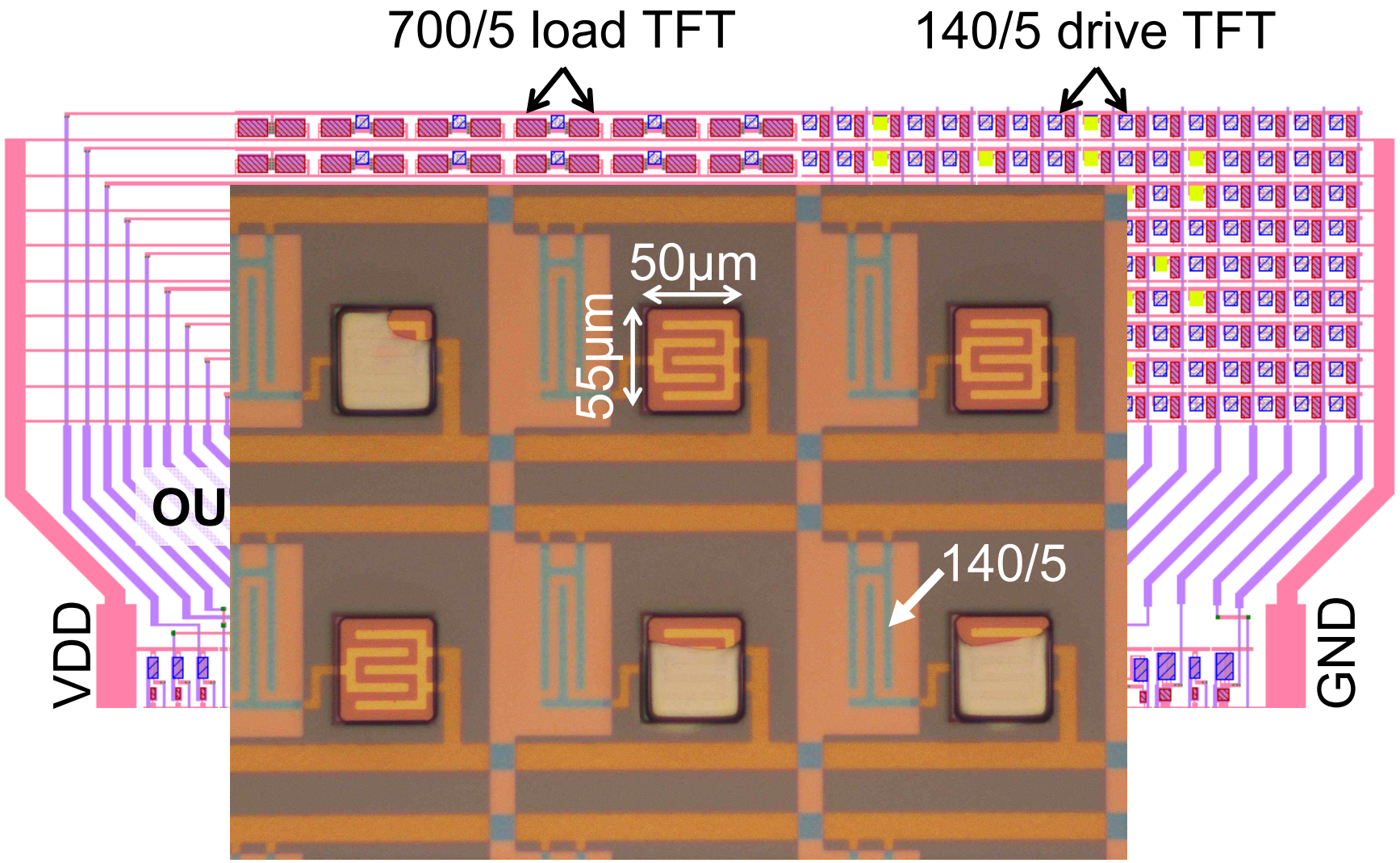




Layout P²ROM chip – NOR array

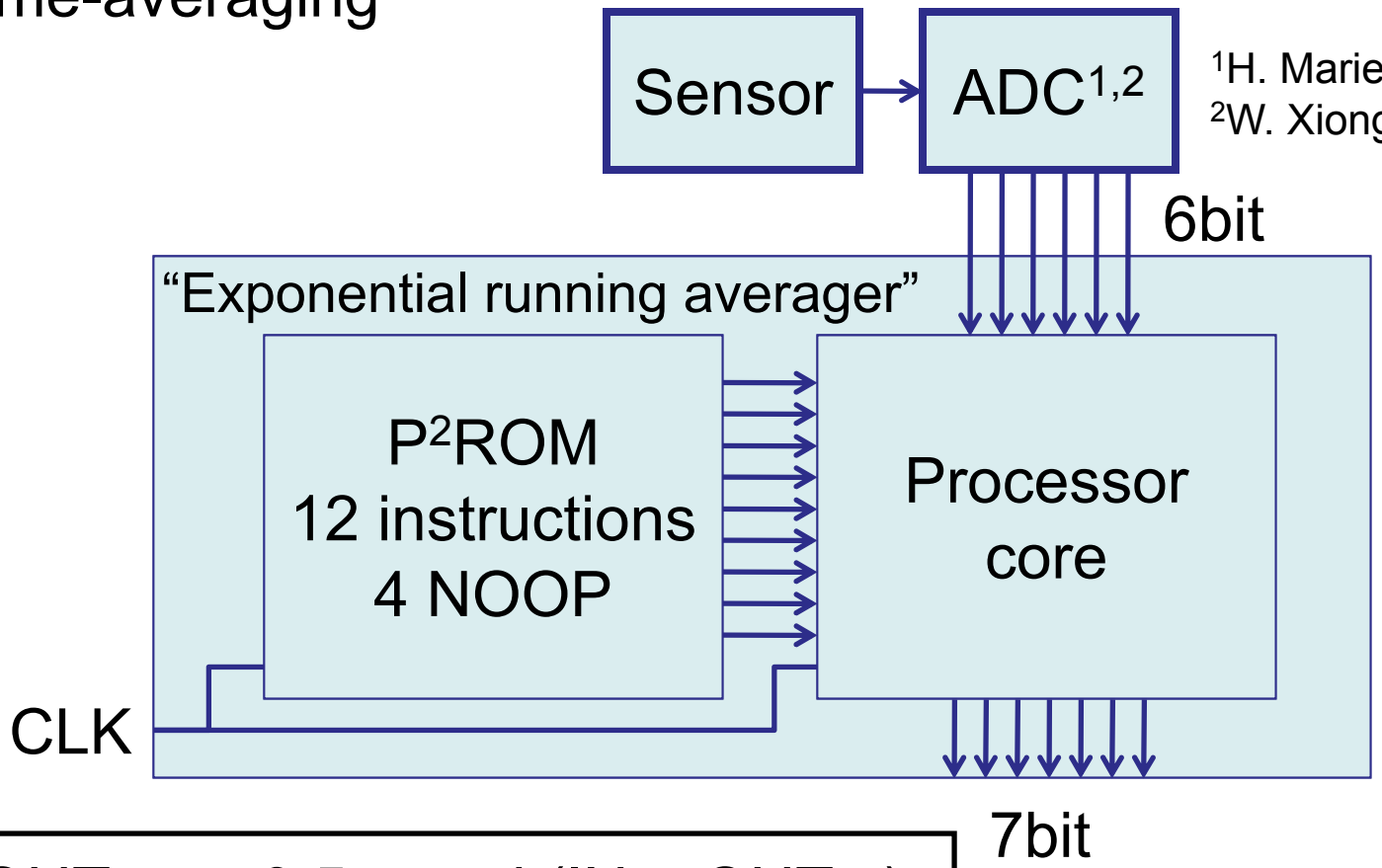


Layout P²ROM chip – NOR array



Exponential running averager

Reduce the random noise of a repetitive digital input by time-averaging

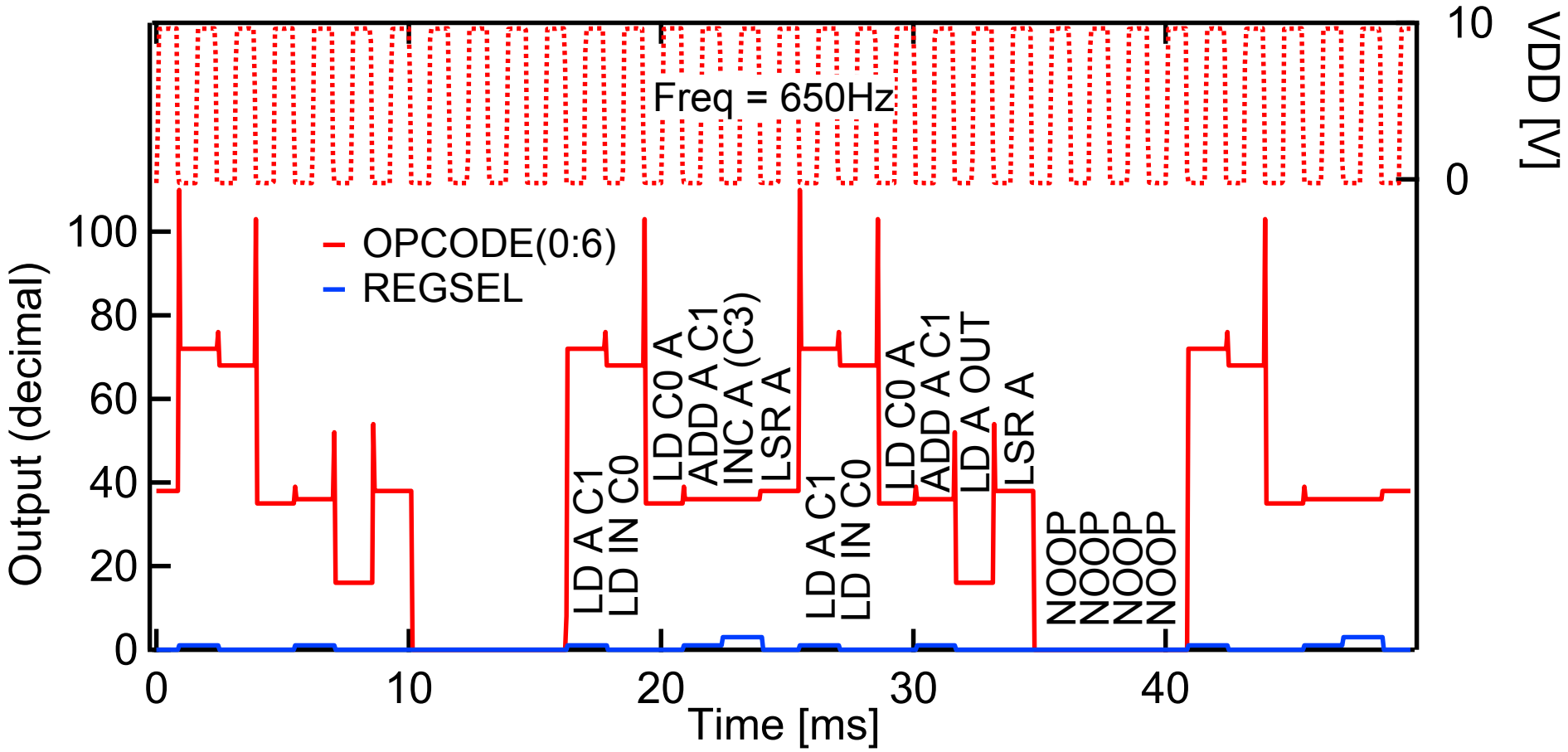


$$OUT_{new} = 0.5 \text{ round } (IN + OUT_{old})$$

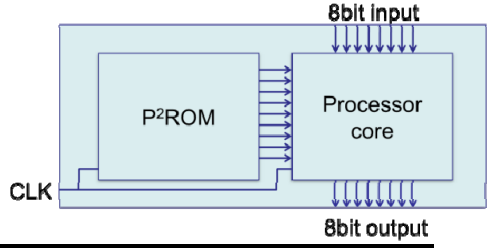
K. Myny *et al.*, ISSCC2011

Measured outputs of P²ROM chip

- Configured as running averager
- 12 instructions + 4 NOOP



Running averager

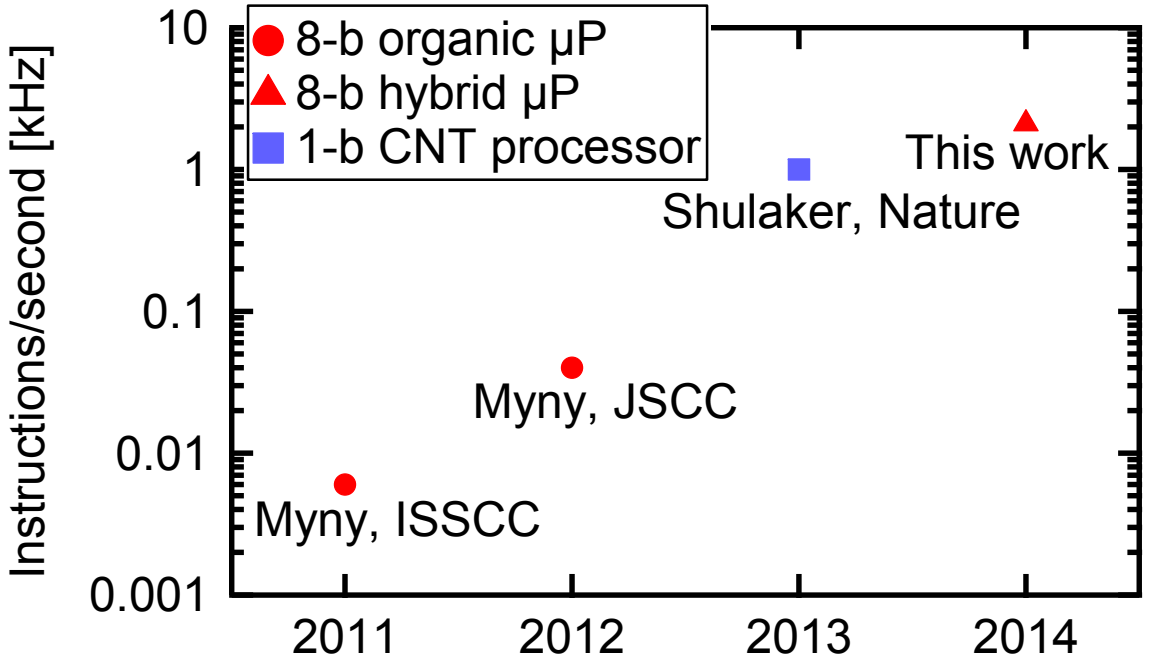


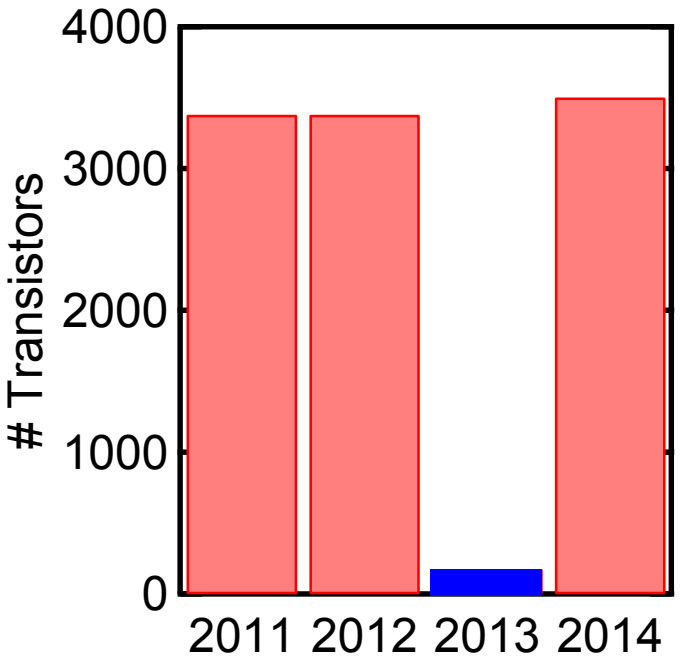
- Combination of processor core and P²ROM chip

Outline

- Introduction
- Technology
- Implementation
  - Processor core chip
  - P^2ROM chip
- Benchmarking
- Conclusions

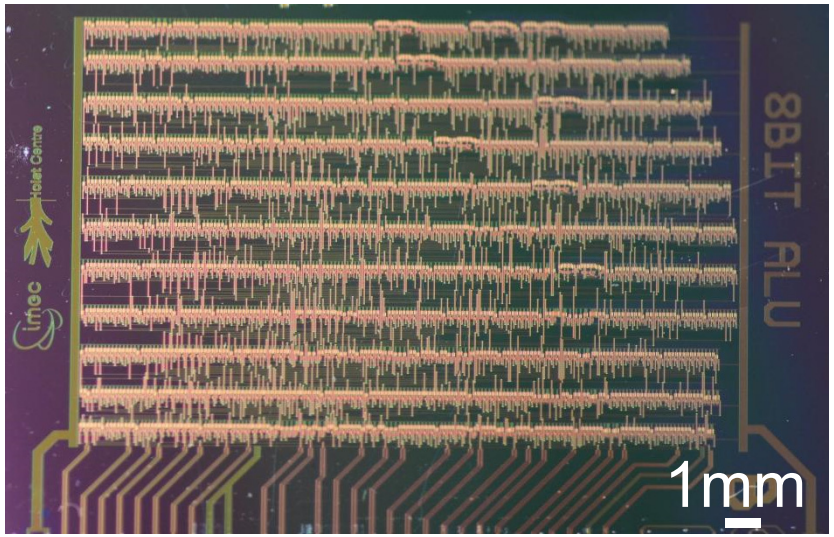
State of art thin-film microprocessor

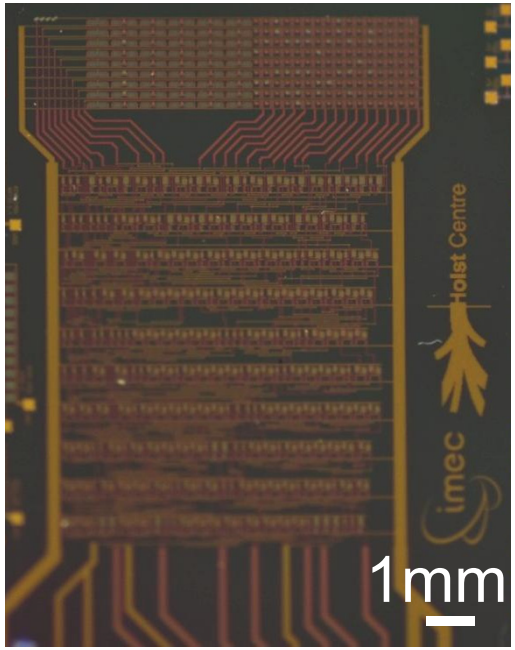




Parameters of both chips

	Processor core	P²ROM
Transistor-count	3504	852 (averager)
Area [cm²]	1.20x1.88 cm²	9.0x6.9 mm²
Pin-count	30	14





Comparison

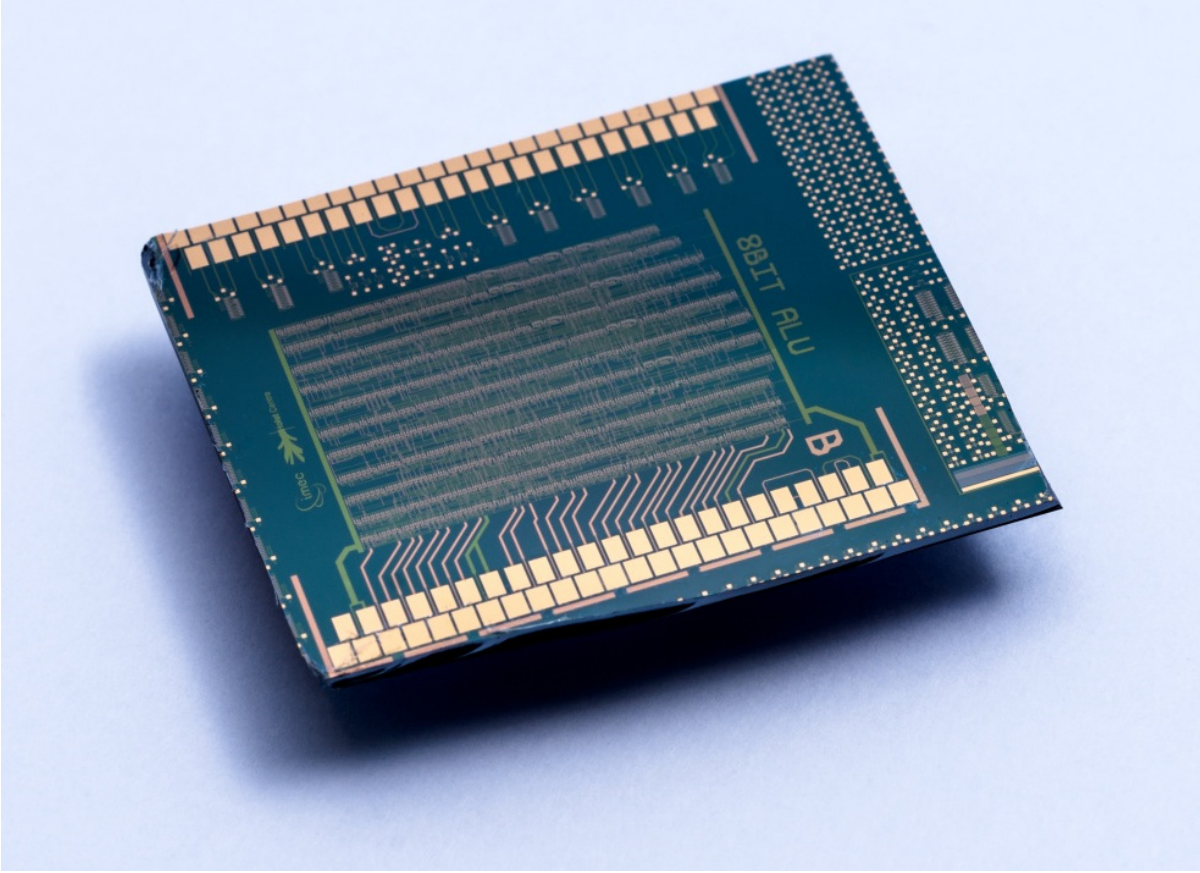
	Organic K. Myny *et al.* JSSC2012	**Hybrid organic/oxide complementary**
Transistor-count processor core	3381	3504
Transistor-count instruction generator	612 (averager)	852 (P^2ROM averager)
Area	1.96 x 1.72 cm^2	1.20 x 1.88 cm^2
Min supply voltage	10V	6.5V
Clock frequency	40Hz @10V VDD	2.1kHz @12V VDD
P-type mobility	~0.15 cm^2/Vs	~0.15 cm^2/Vs (p-TFT) ~ 2.00 cm^2/Vs (n-TFT)
Logic family	Unipolar p-type	Complementary
Technology	5 µm	5 µm
Bus width	8 bit	8 bit

Conclusions

- A hybrid organic-oxide thin-film microprocessor has been demonstrated, exceeding state-of-art
- Main improvements on the processor core chip:
  - Signal buffering
  - Mirror adder
  - Extended standard cell library
- P^2ROM memory has been introduced
  - Print-programmable memory
  - Configurable instruction generator
- Successful integration of averager P^2ROM and processor core chip

Acknowlegdements

- This work was performed in collaboration between IMEC and TNO in the frame of the HOLST Centre



Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption

J. Genoe[1,2], K. Obata[3], M. Ameys[1], K. Myny[1], T.H. Ke[1], M. Nag[1,2], S. Steudel[1], S. Schols[1], J. Maas[4], A. Tripathi[4], J.-L. van der Steen[4], T. Ellis[4], G.H. Gelinck[4], and P. Heremans[1,2,4]

1 imec 2 KU LEUVEN 3 Panasonic 4 Holst Centre
Open Innovation by IMEC and TNO

	1965-75	1975-85	1985-95	1995-2005	2005-2015	2015-X
						?
after J.P.Morgan	mainframe	Mini computer	PC	Notebooks	Mobile internet	Next

# sold	1M	10M	100M	1B	10B	100B
Volume [m^3]	10	1	0.1	0.01	0.001	0.0001
Total [Mm^3]	10	10	10	10	10	10

Future devices beyond the tablet:

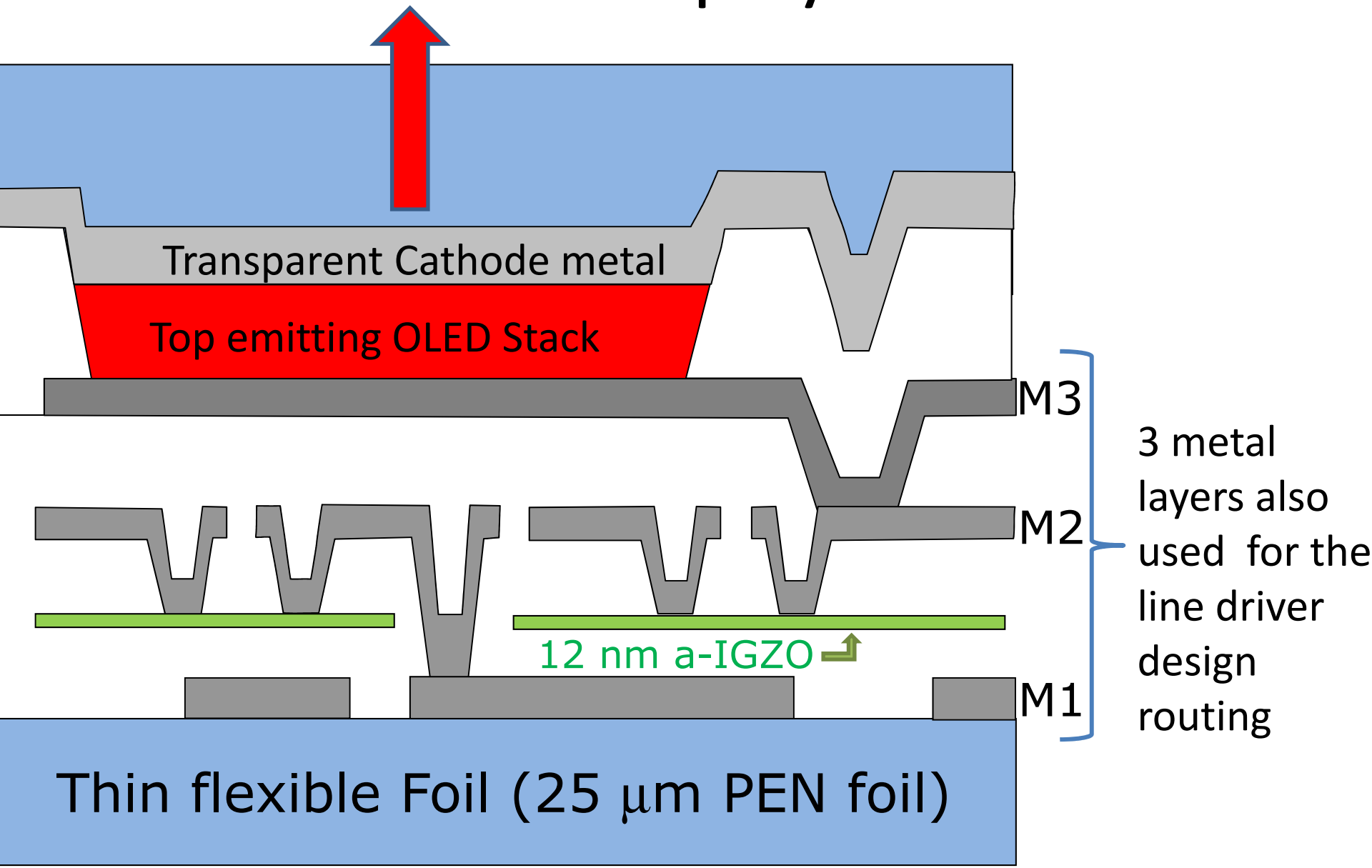
- 10 times lower volume
- 10 times lower weight
- Display size equal or larger than the device

→ Foil-based future displays

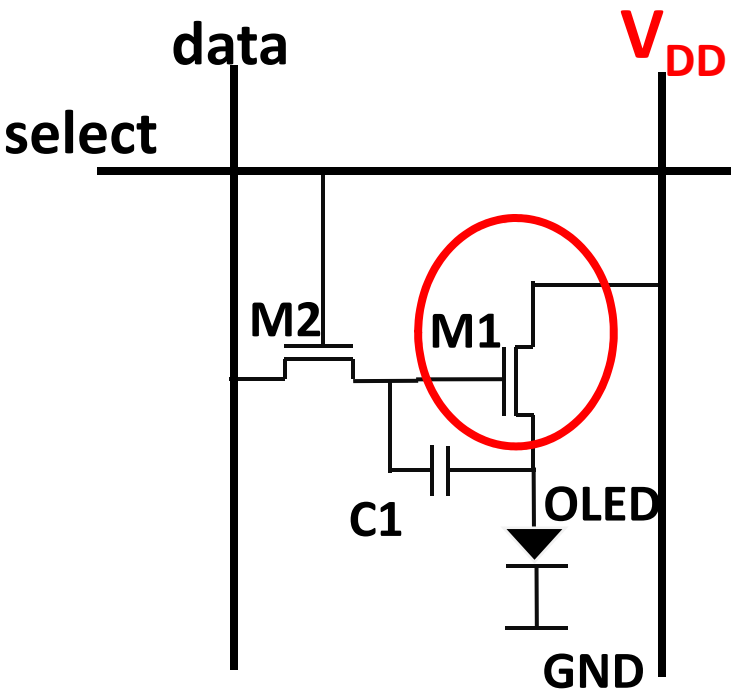
Requirements of future displays

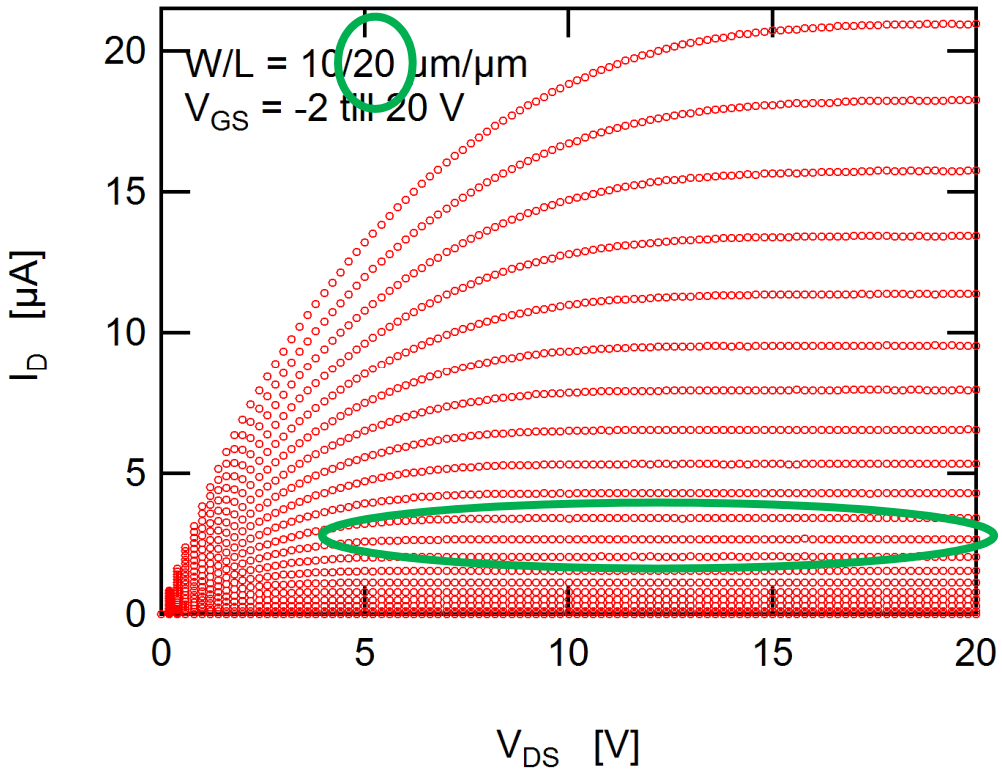
- Ultra thin
- Ultra light
- Unbreakable
- Flexible, foldable or rollable
- Low-power
- High resolution (> 500 dpi)
- High color quality

AMOLED displays on foil



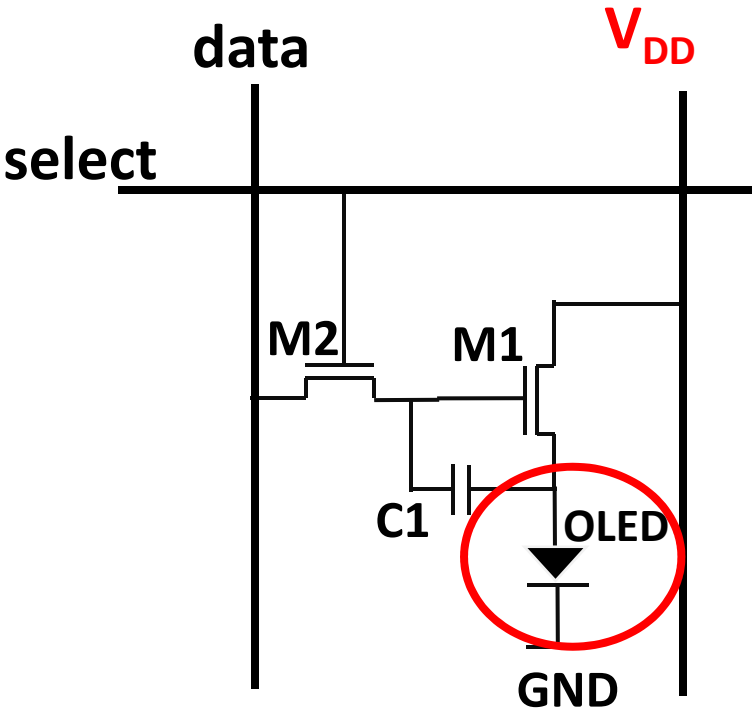
Driving transistor (M1)





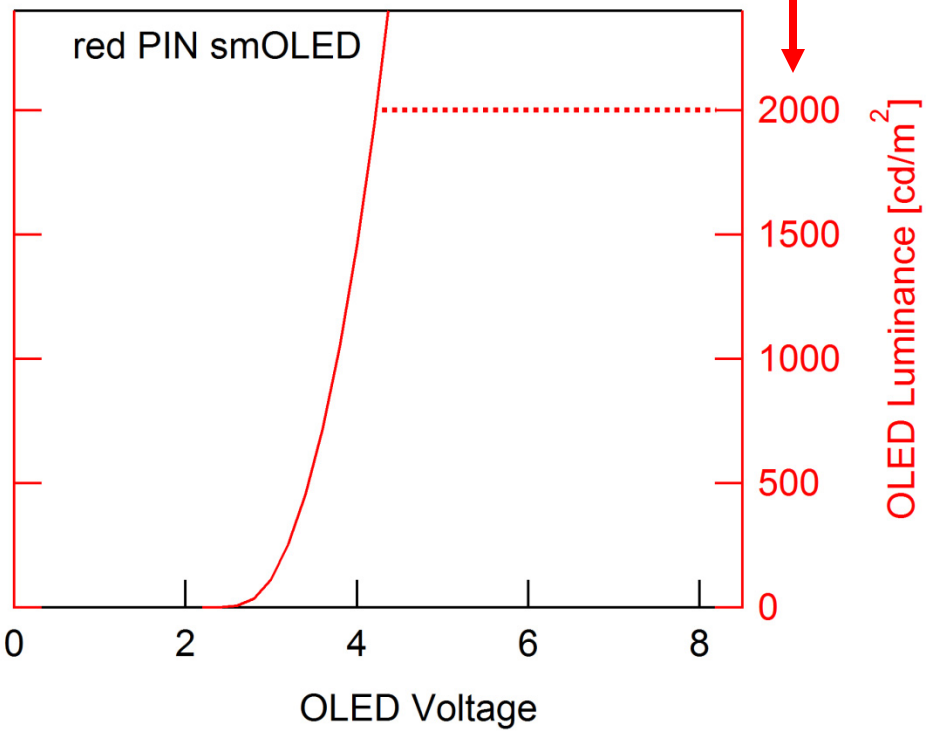
$V_{DS} > V_{GS}-V_T$

Pixel power loss

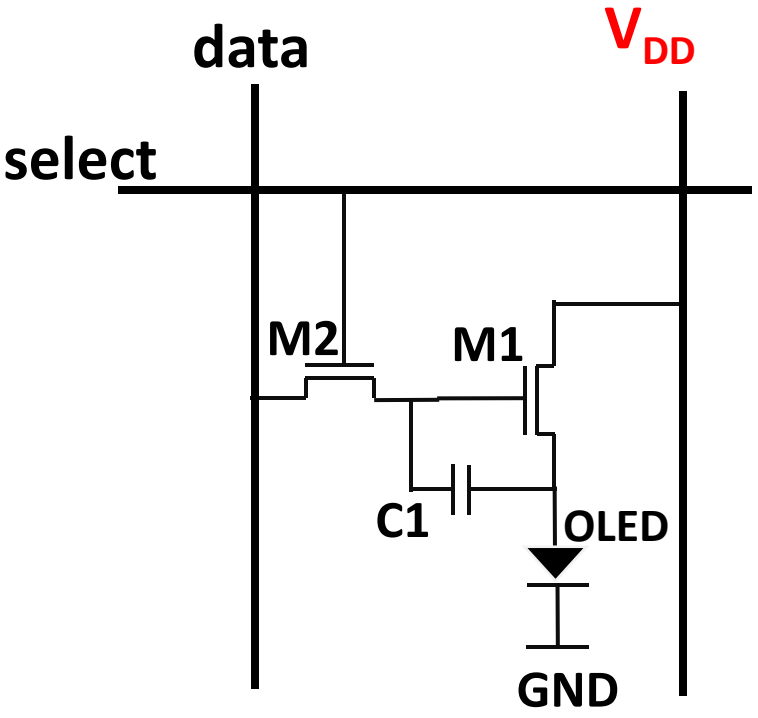


Classical approach on flex

2000Cd/m²

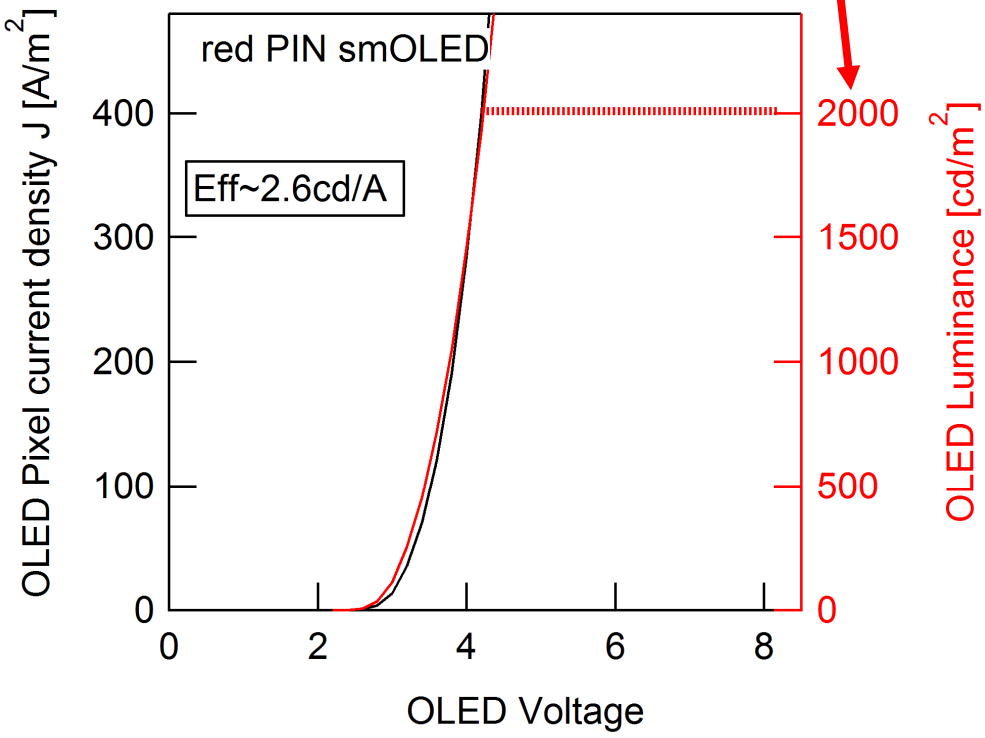


Pixel power loss

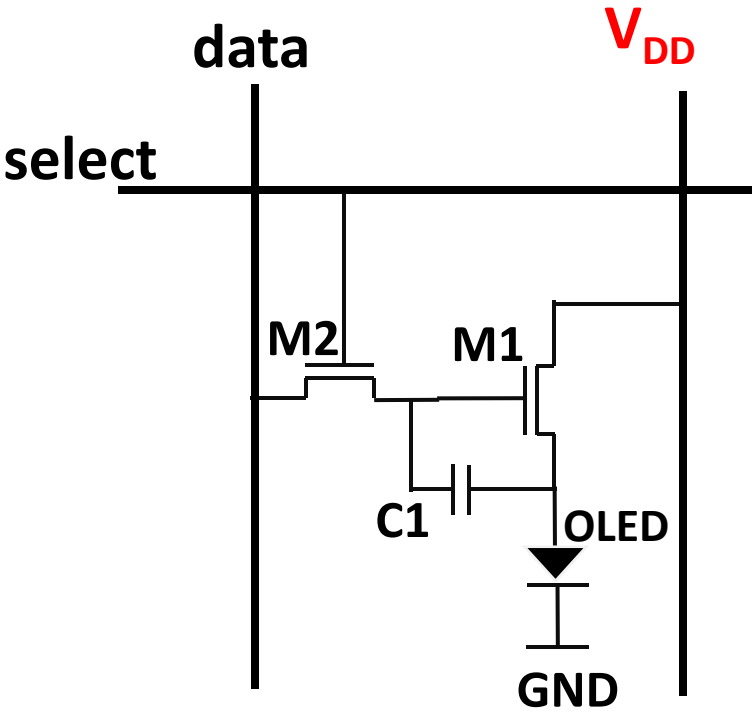


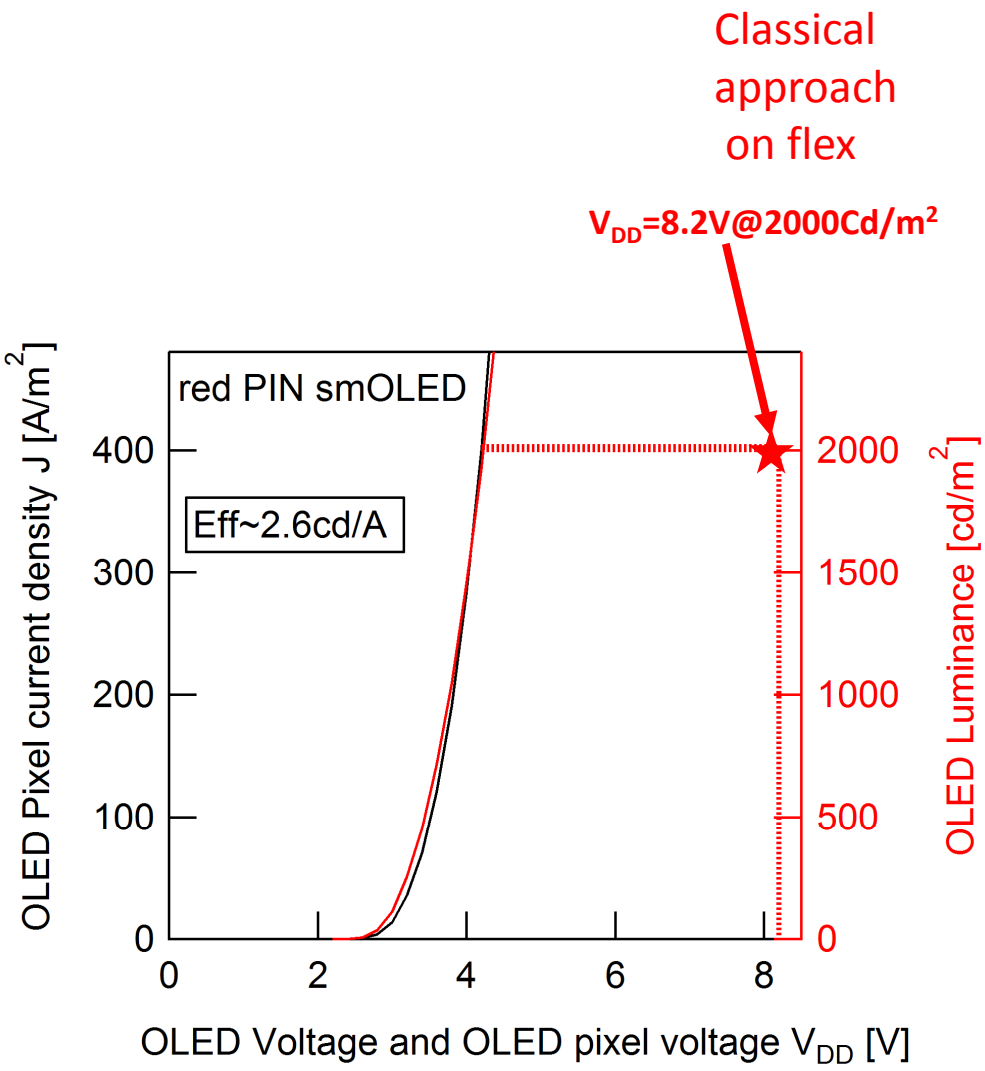
Classical approach on flex

2000Cd/m²



Pixel power loss

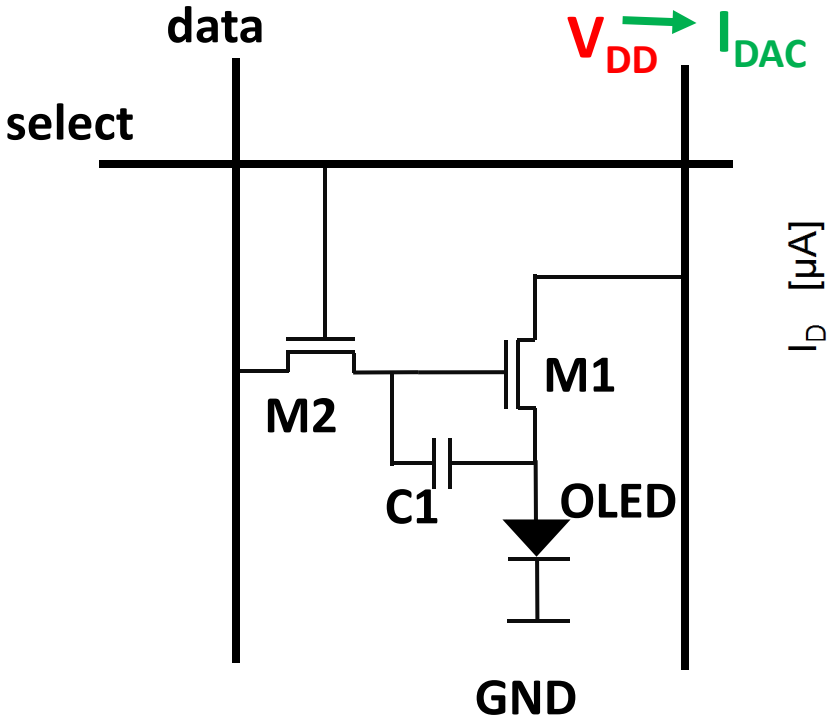


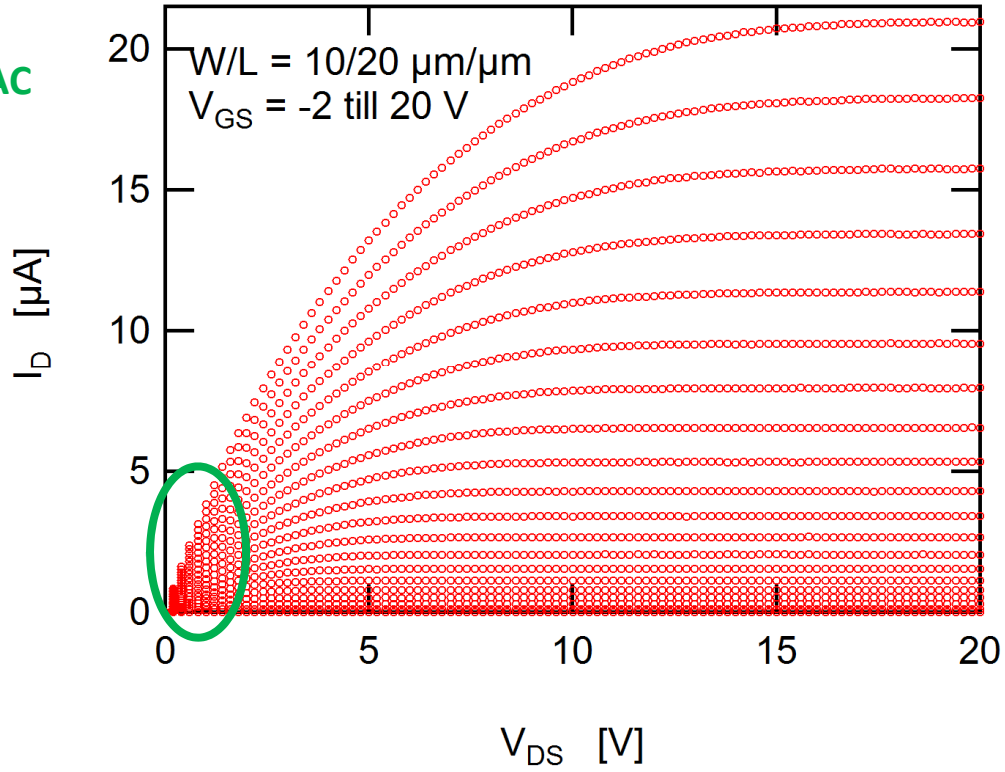


Outline

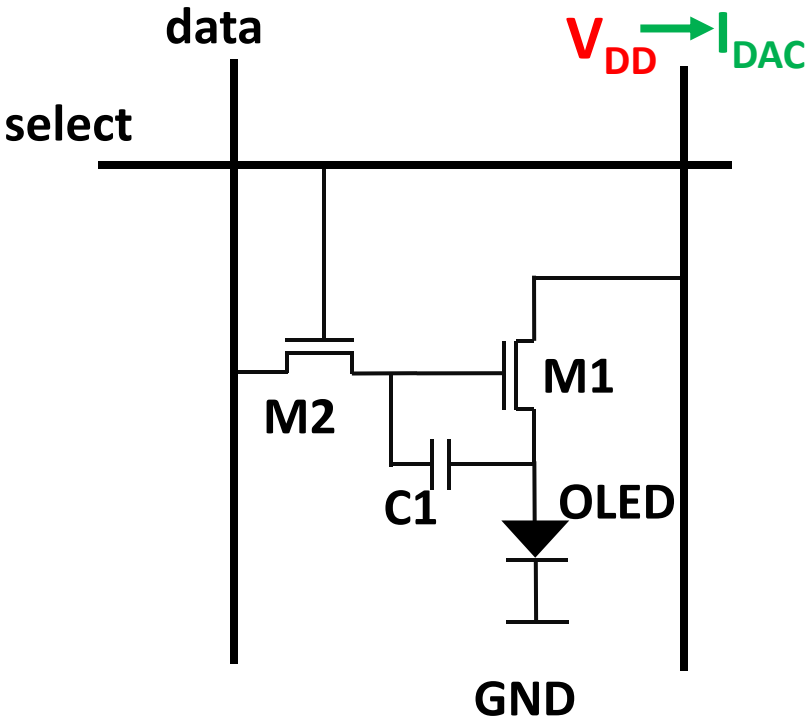
- Flexible display targets
- Putting the external silicon into current control
- Selected Pulse width modulation
- Multiplexed scan line drivers
- Display integration
- Conclusions

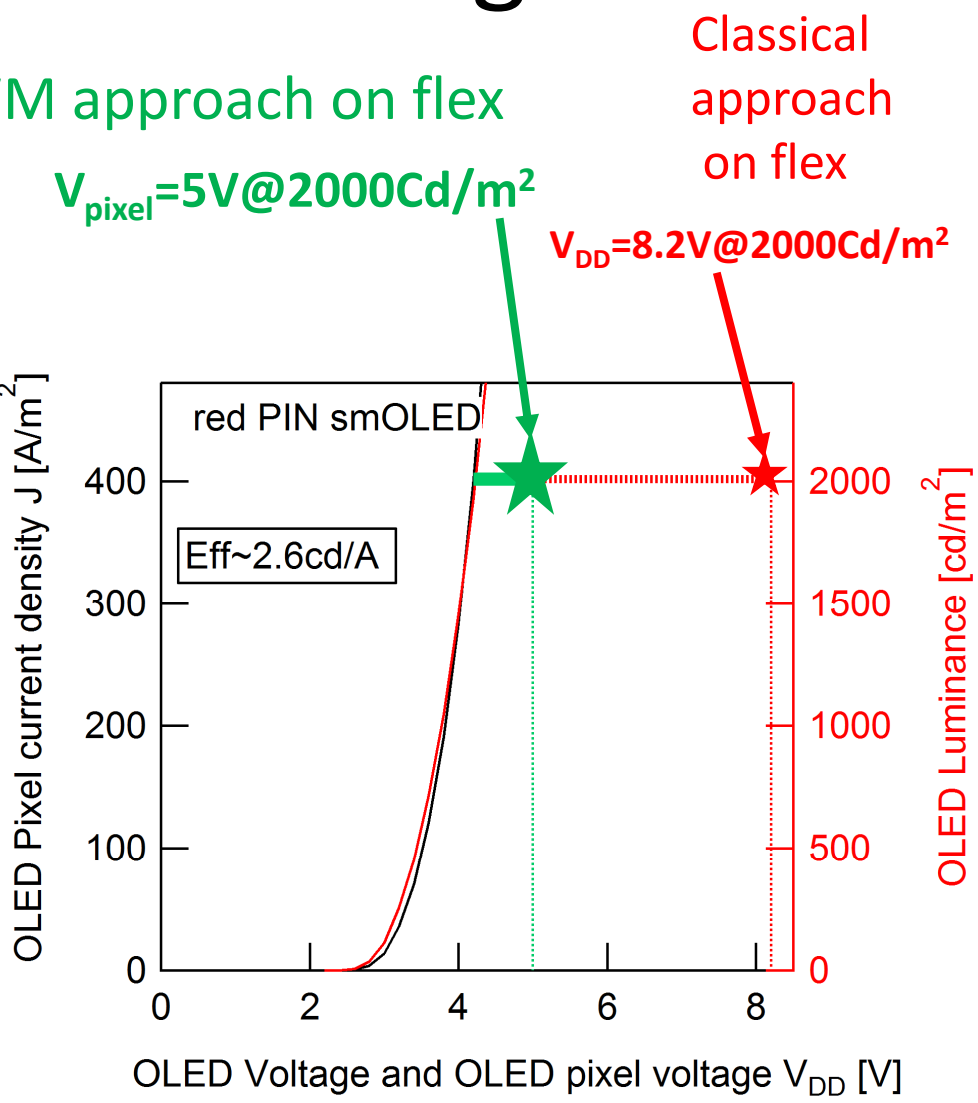
Linear regime driving



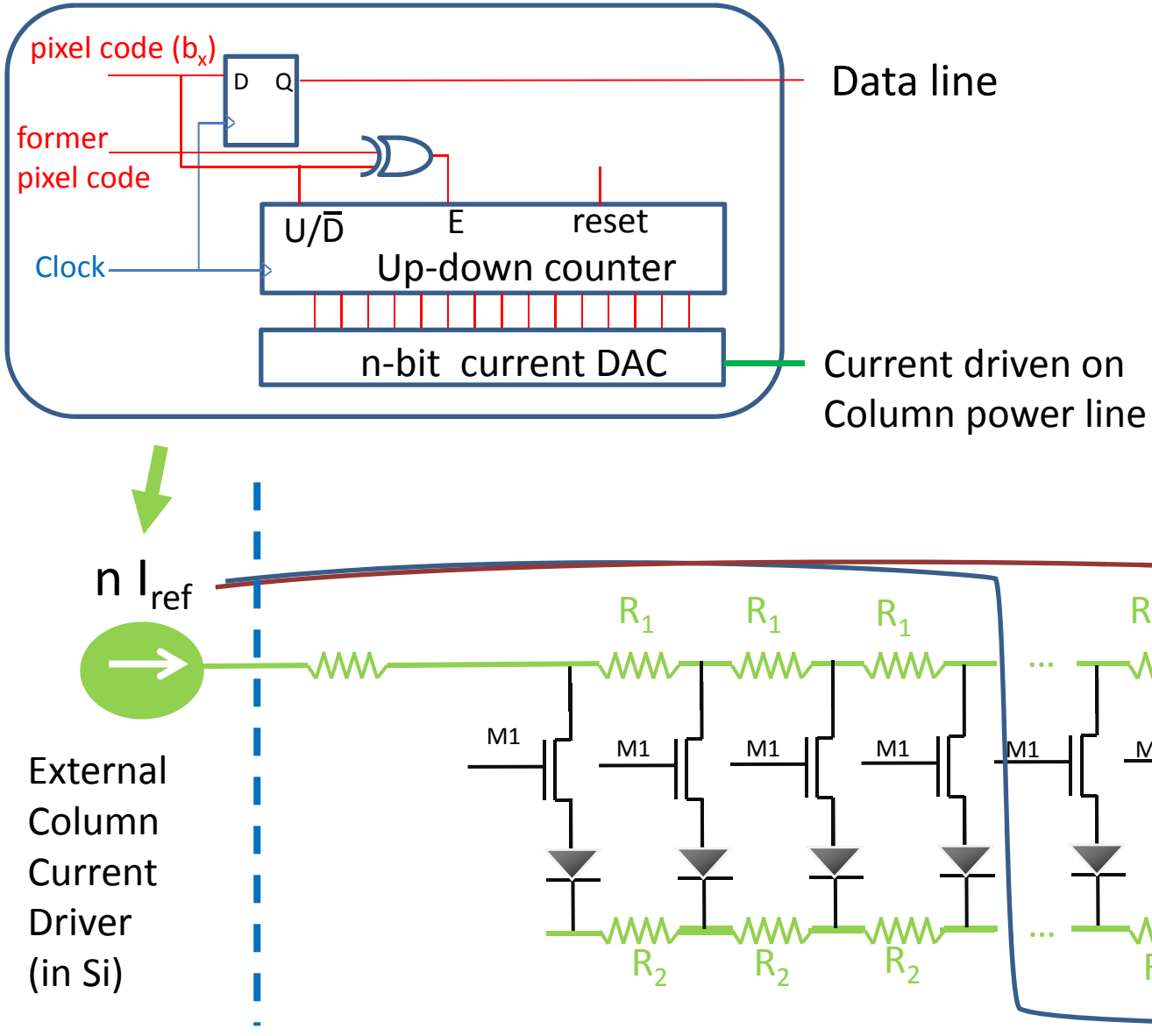


Linear regime driving





Silicon current driving

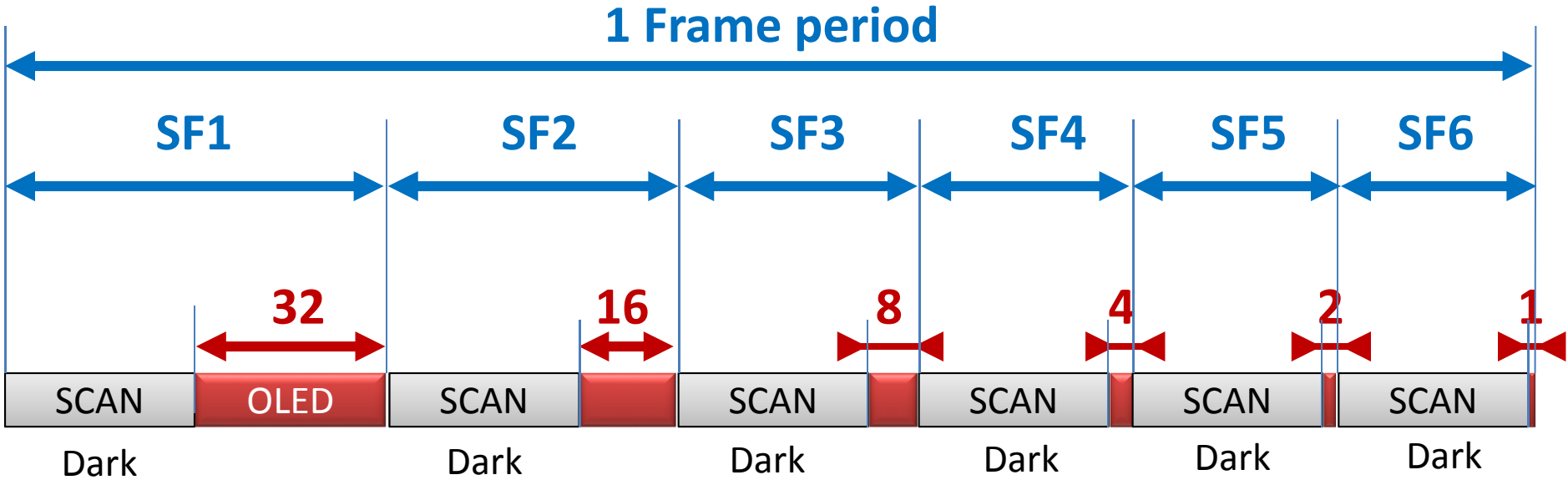


Outline

- Flexible display targets
- Putting the external silicon into current control
- Selected Pulse Width Modulation
- Multiplexed scan line drivers
- Display integration
- Conclusions

Classical PWM for displays

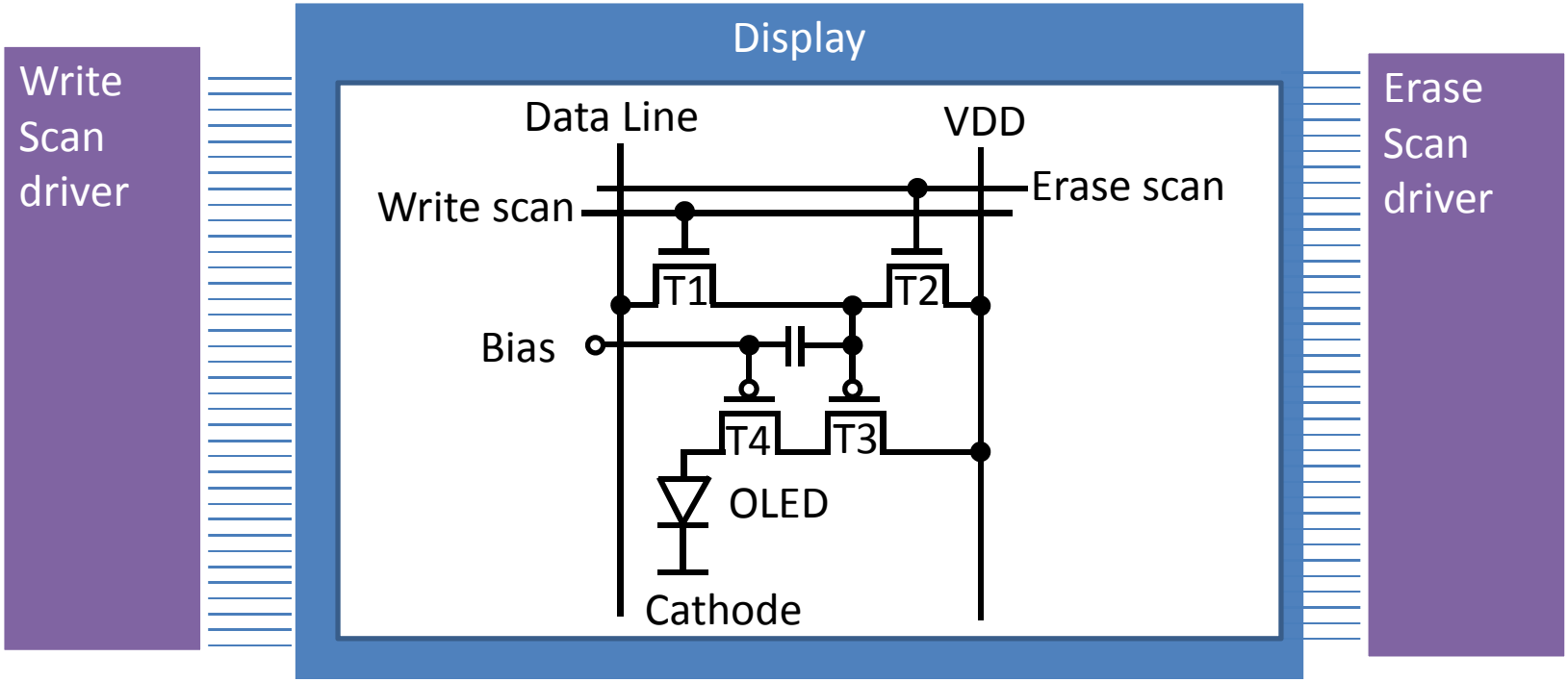
[1] M. Mizukami, et al., “6-bit digital VGA OLED,” Tech. Dig. SID 31, 912 (2000).



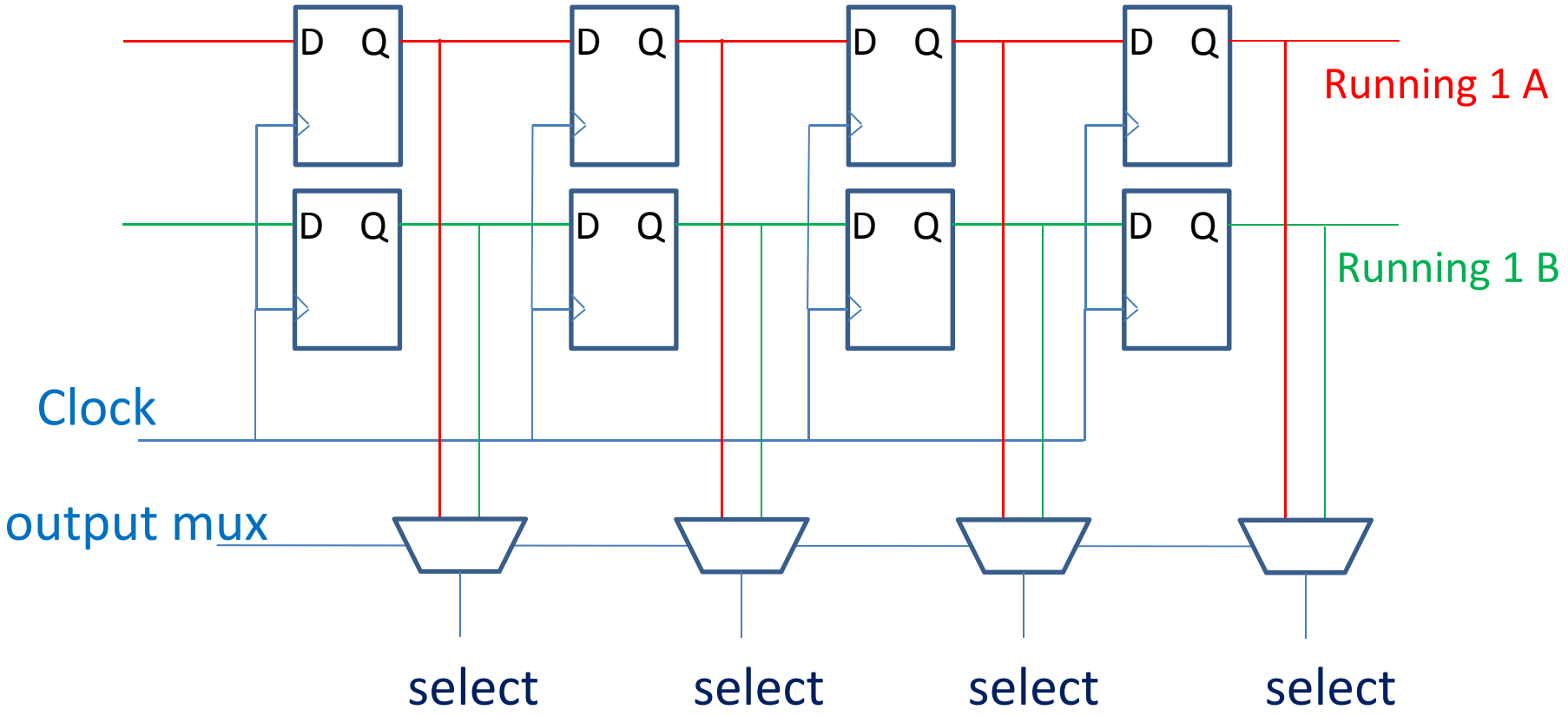
- **The time scanning through the pixels is larger than the time the OLED is on.**
- **This gets worse, when the number of grey scales further increases.**

Double scan lines

[2] Y. Tanada, et al., "A 4.3-in. VGA (188 ppi) AMOLED display with a new driving method," Tech. Dig. SID 35, 1398 (2004).



Multiplexed scan lines



Possible coding scheme

Subframe number (part α, β)	bit driven after the first select line gets active	bit driven after the second select line gets active
1 (1, 31)	b_0	0
2 (2, 30)	b_1	0
3 (4, 28)	b_2	0
4 (8, 24)	b_3	0
5 (16, 16)	b_4	0
6 (32, /)	b_5	/
7 (64, /)	b_6	/
8 (128, /)	b_7	/

384 pulses

Possible coding scheme

Subframe number (part α, β)	bit driven after the first select line gets active	bit driven after the second select line gets active
1 (1, 31)	b_0	0
2 (2, 30)	b_1	0
3 (4, 28)	b_2	0
4 (8, 24)	b_3	0
5 (16, 16)	b_4	0
6 (32, /)	b_5	/
7 (64, /)	b_6	/
8 (128, /)	b_7	/

384 pulses

Improved coding scheme

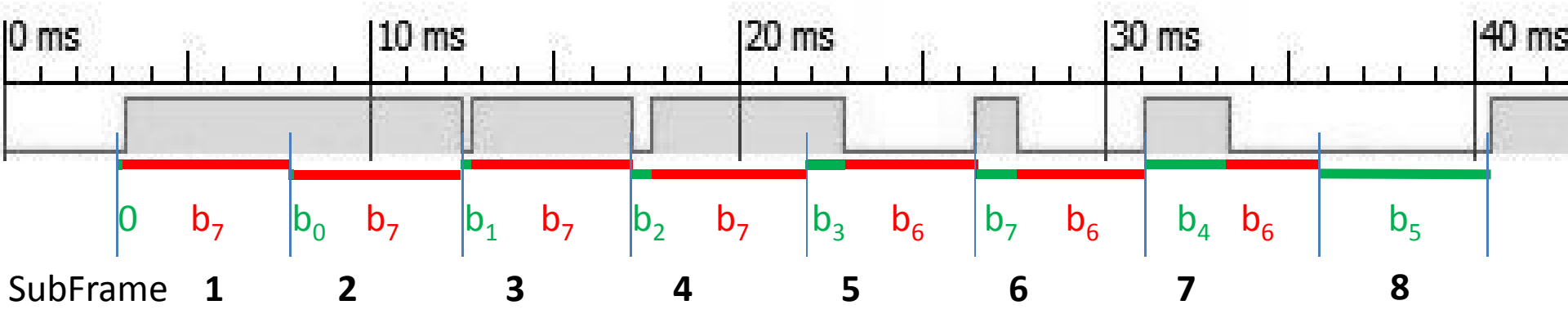
Subframe number (part α, β)	bit driven after the first select line gets active	bit driven after the second select line gets active
1 (1, 31)	0	b_7
2 (1, 31)	b_0	b_7
3 (2, 30)	b_1	b_7
4 (4, 28)	b_2	b_7
5 (8, 24)	b_3	b_6
6 (8, 24)	b_7	b_6
7 (16, 16)	b_4	b_6
8 (32, /)	b_5	/

256 pulses

Improved coding scheme

Subframe number (part α, β)	bit driven after the first select line gets active	bit driven after the second select line gets active
1 (10, 310)	0	b_7
2 (10, 310)	b_0	b_7
3 (20, 300)	b_1	b_7
4 (40, 280)	b_2	b_7
5 (80, 240)	b_3	b_6
6 (80, 240)	b_7	b_6
7 (160, 160)	b_4	b_6
8 (320, /)	b_5	/

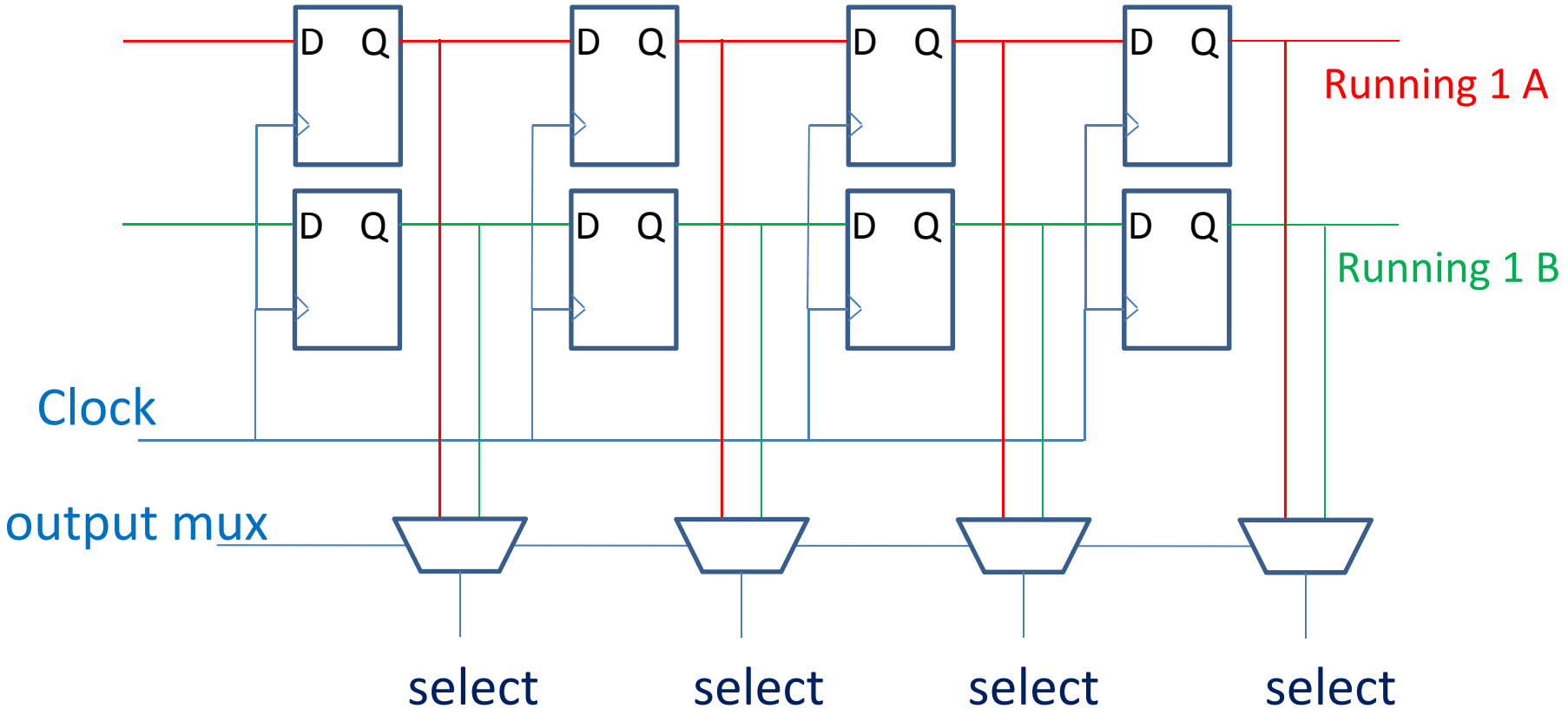
Subframe number (part α, β)	bit driven after the first select line gets active	bit driven after the second select line gets active
1 (10, 310)	0	b_7
2 (10, 310)	b_0	b_7
3 (20, 300)	b_1	b_7
4 (40, 280)	b_2	b_7
5 (80, 240)	b_3	b_6
6 (80, 240)	b_7	b_6
7 (160, 160)	b_4	b_6
8 (320, /)	b_5	/



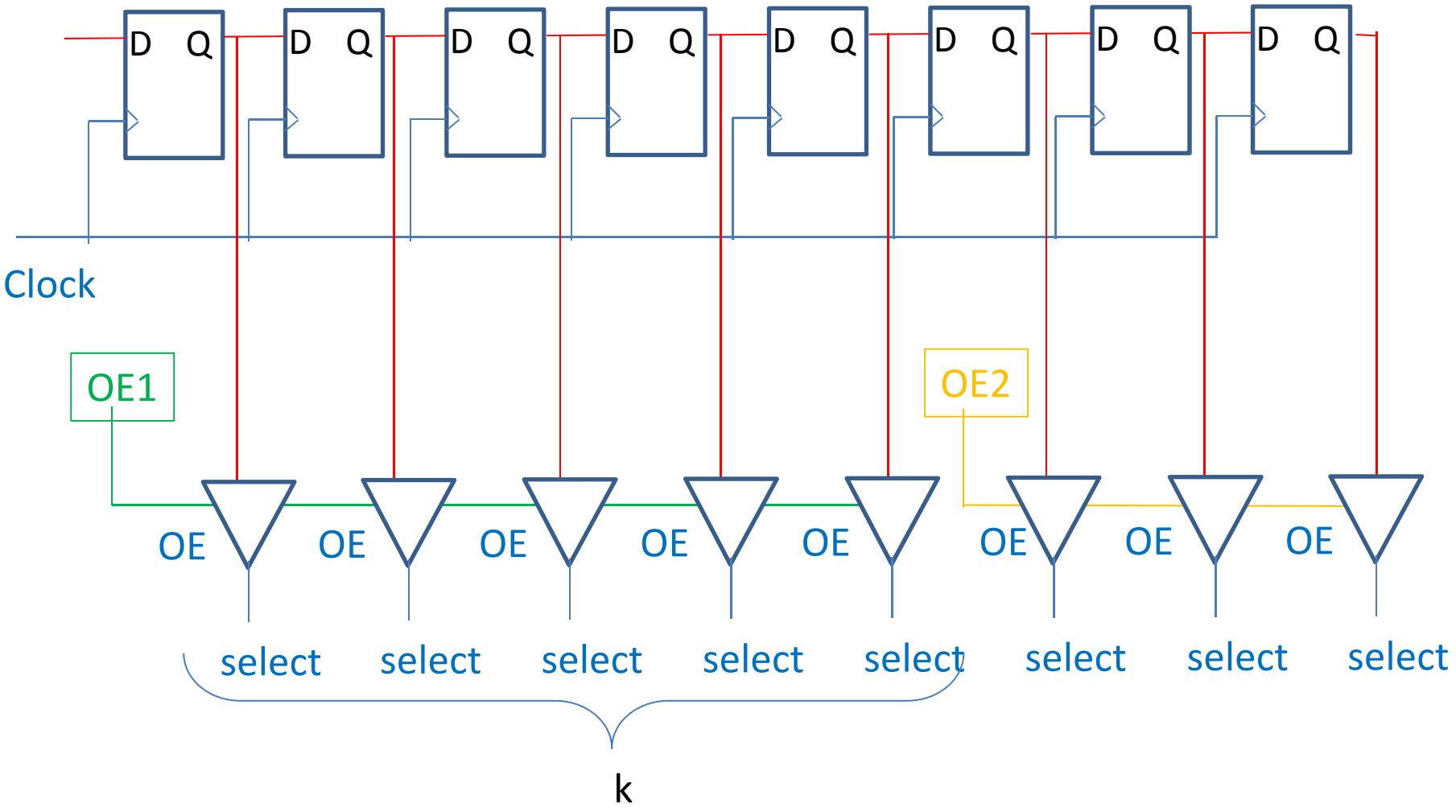
Outline

- Flexible display targets
- Putting the external silicon into current control
- Selected Pulse width modulation
- Multiplexed scan line drivers
- Display integration
- Conclusions

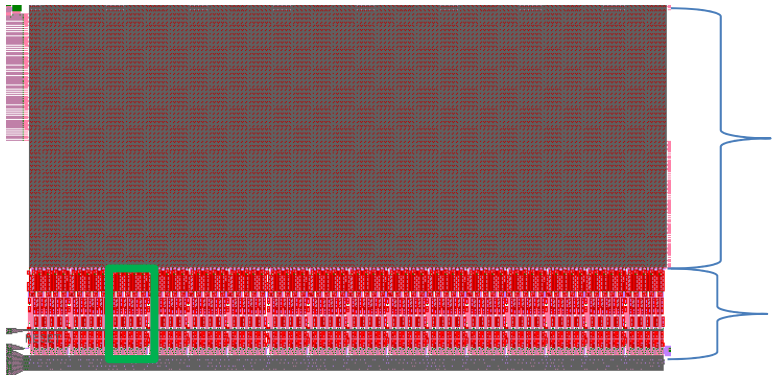
Multiplexed scan line drivers



Output enable signals

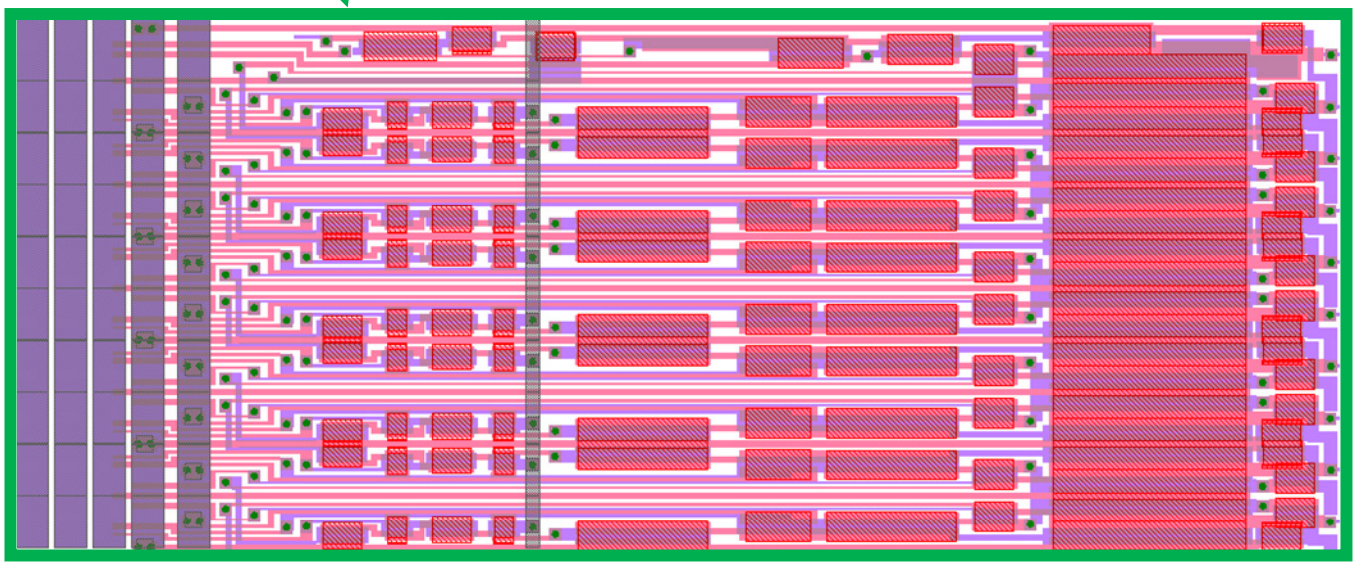


Display layout



64*160 pixels [80 µm * 80 µm]
Total size: 5.1 mm*12.8 mm

16 blocks of 10 line drivers
Total size: 2.0 mm*12.8 mm

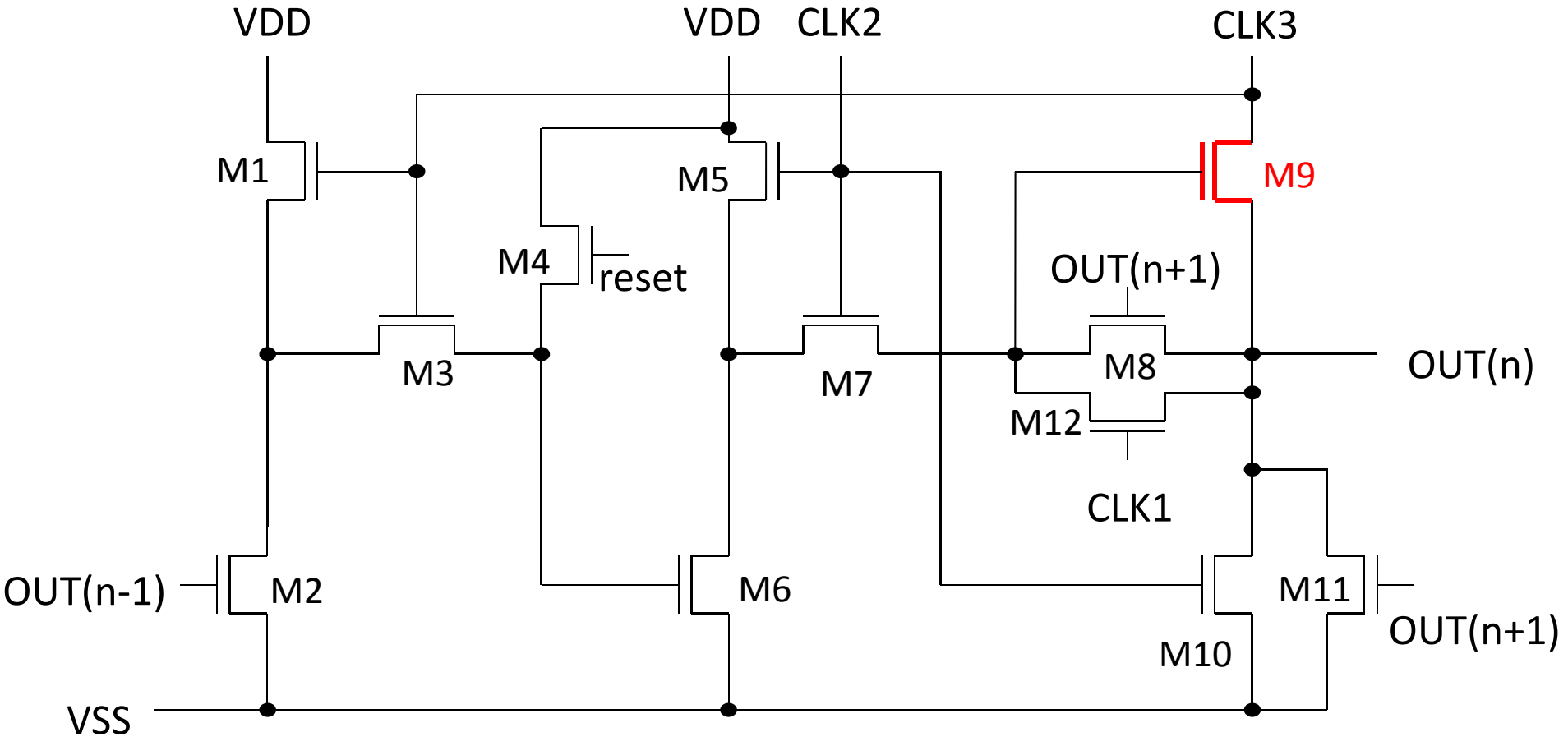


80 µm

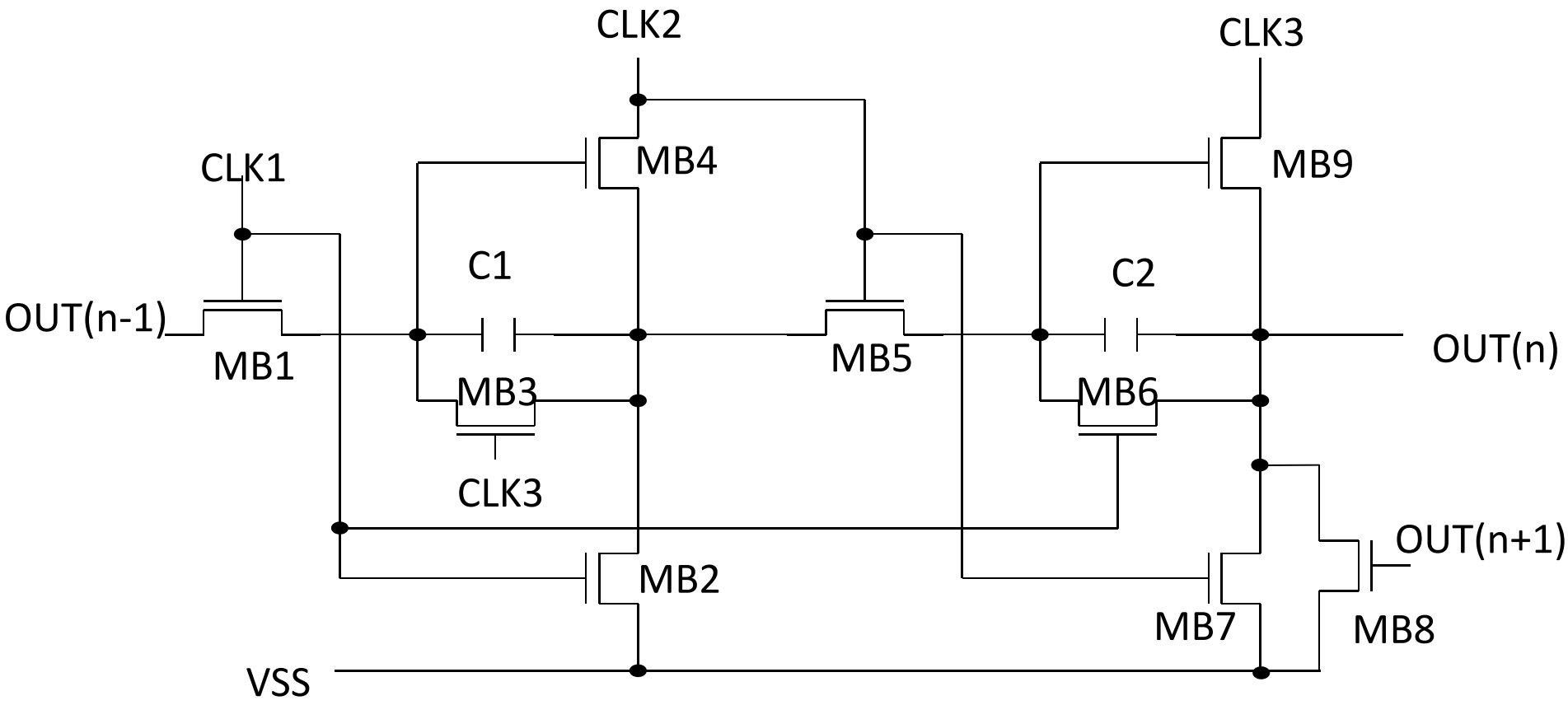
2 clk delay line driver (1 instance)
A B

3 clk delay line driver (9 instances)
A BC

Schematic 3 clock line driver

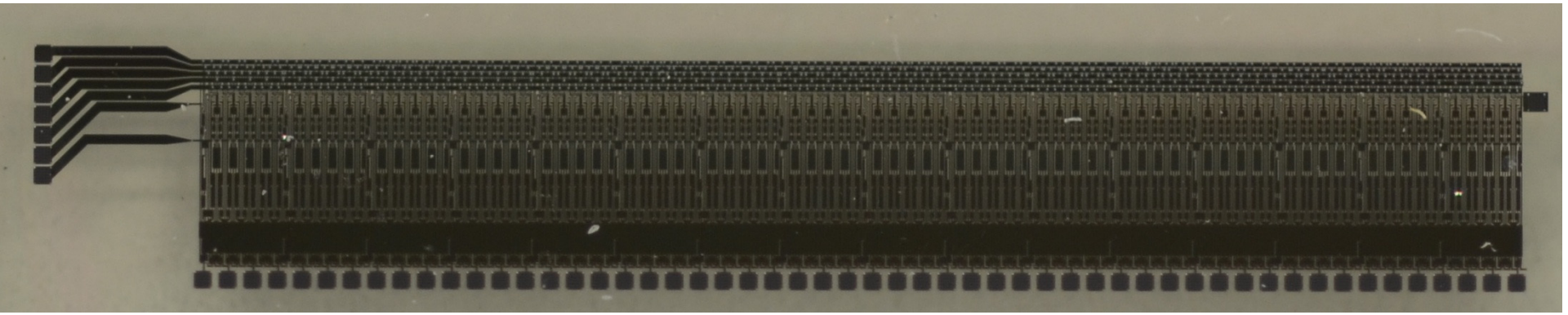


Schematic 2 clock line driver



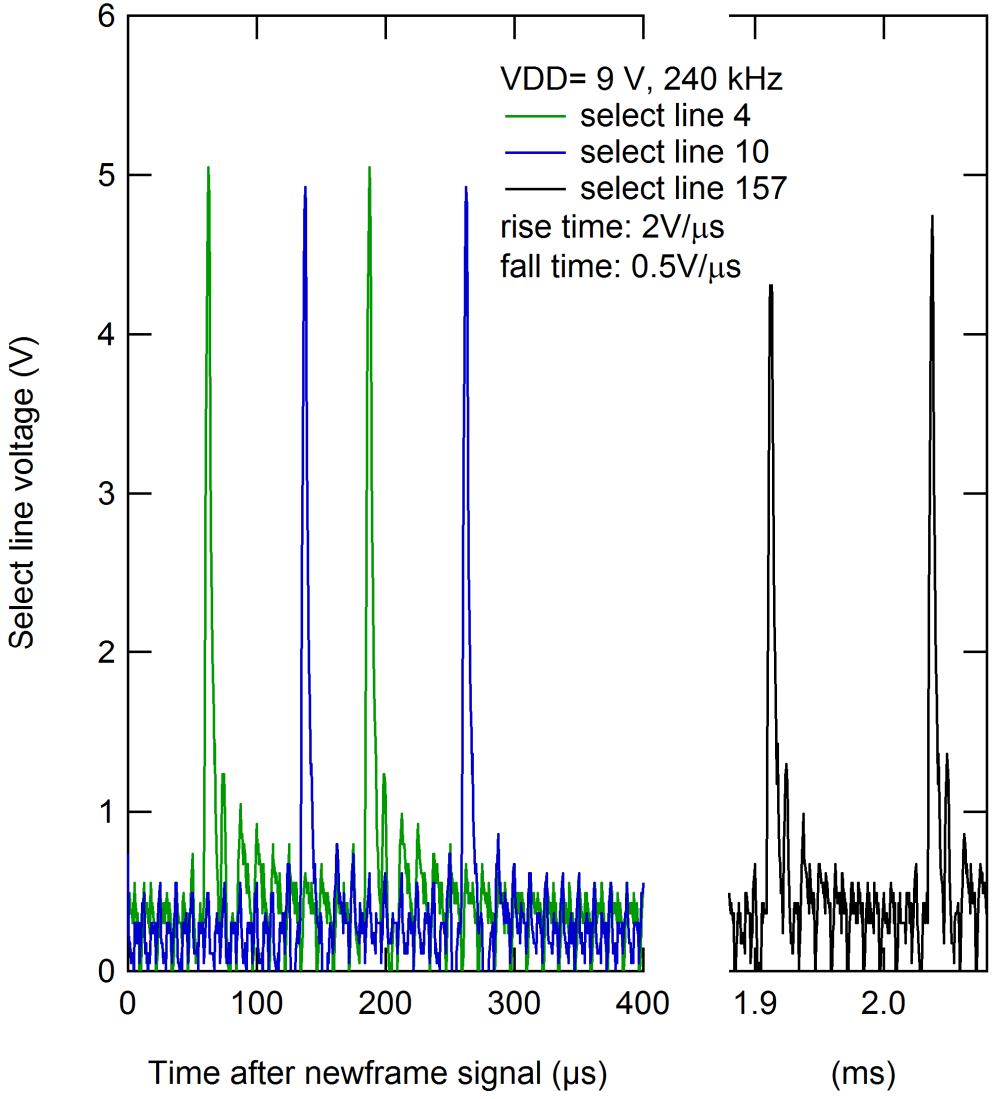
Implementation line driver

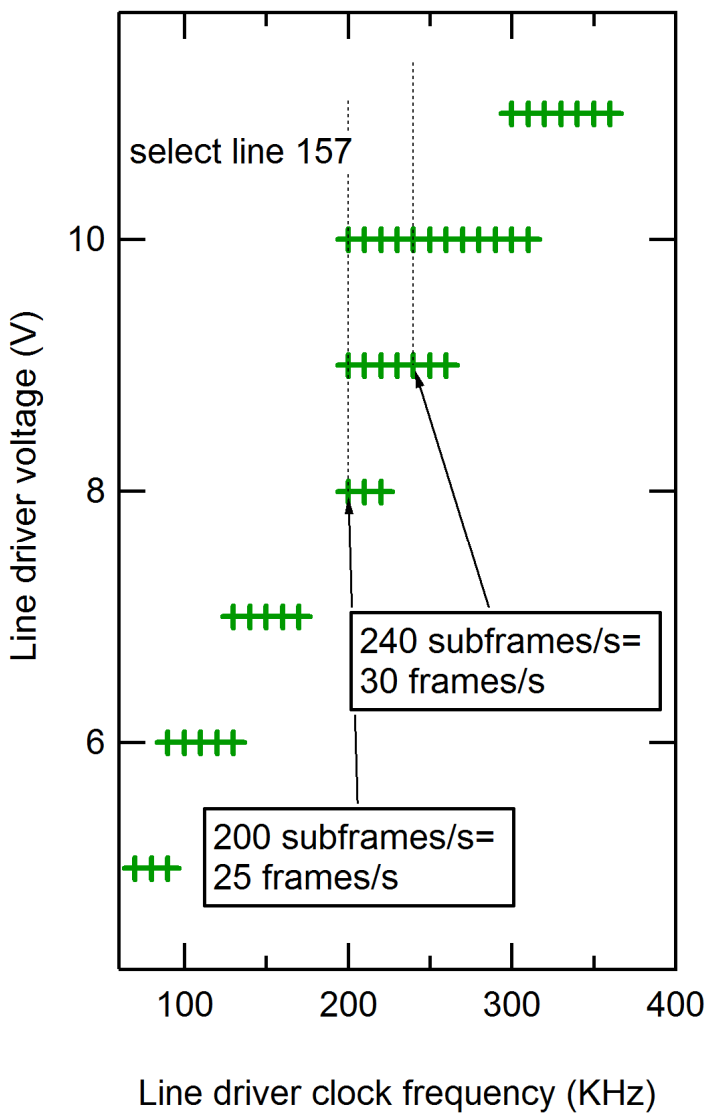
Die picture individual line driver



16 blocks of 10 line drivers
Total size: 2.0 mm*12.8 mm

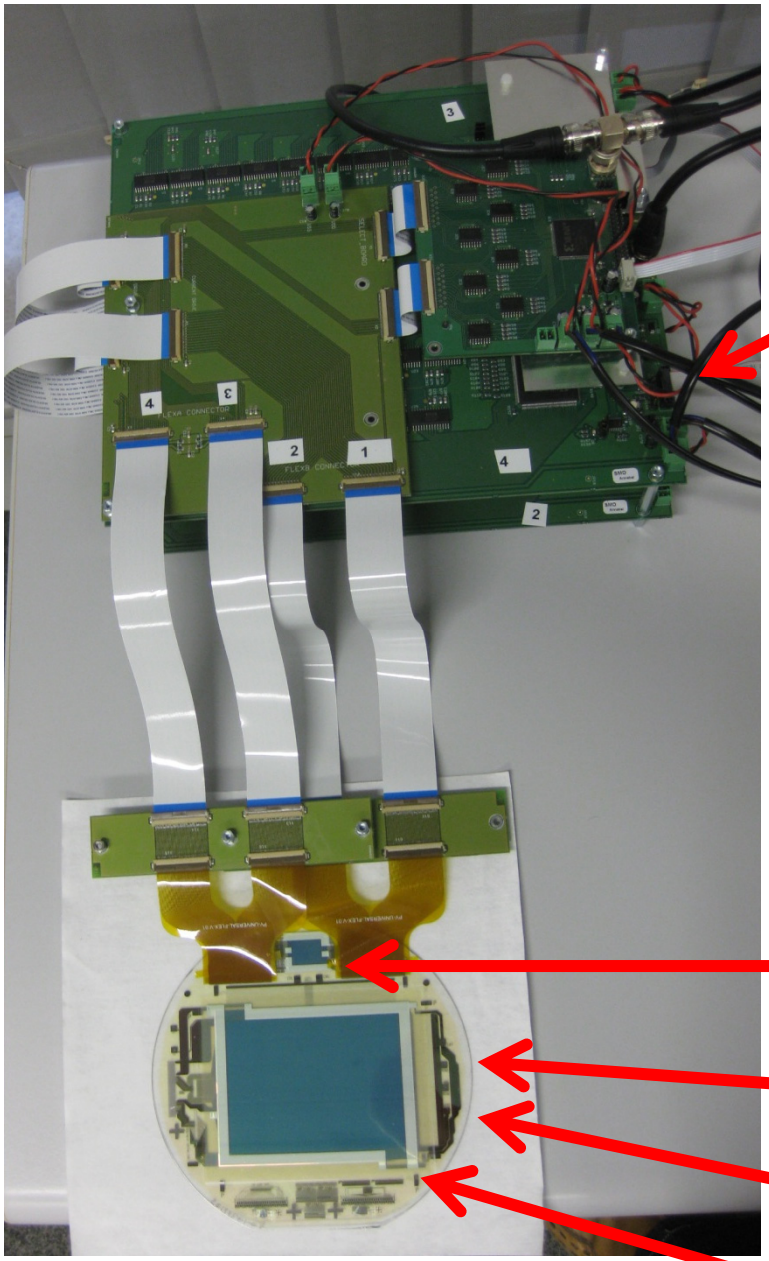
Characterization line driver



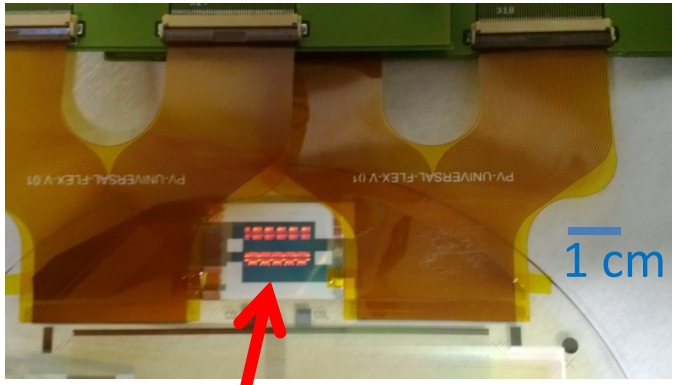


Outline

- Flexible display targets
- Putting the external silicon into current control
- Selected Pulse width modulation
- Multiplexed scan line drivers
- Display integration
- Conclusions



Digital current driving PCBs comprising 64 individual current DACs and 5 FPGAs



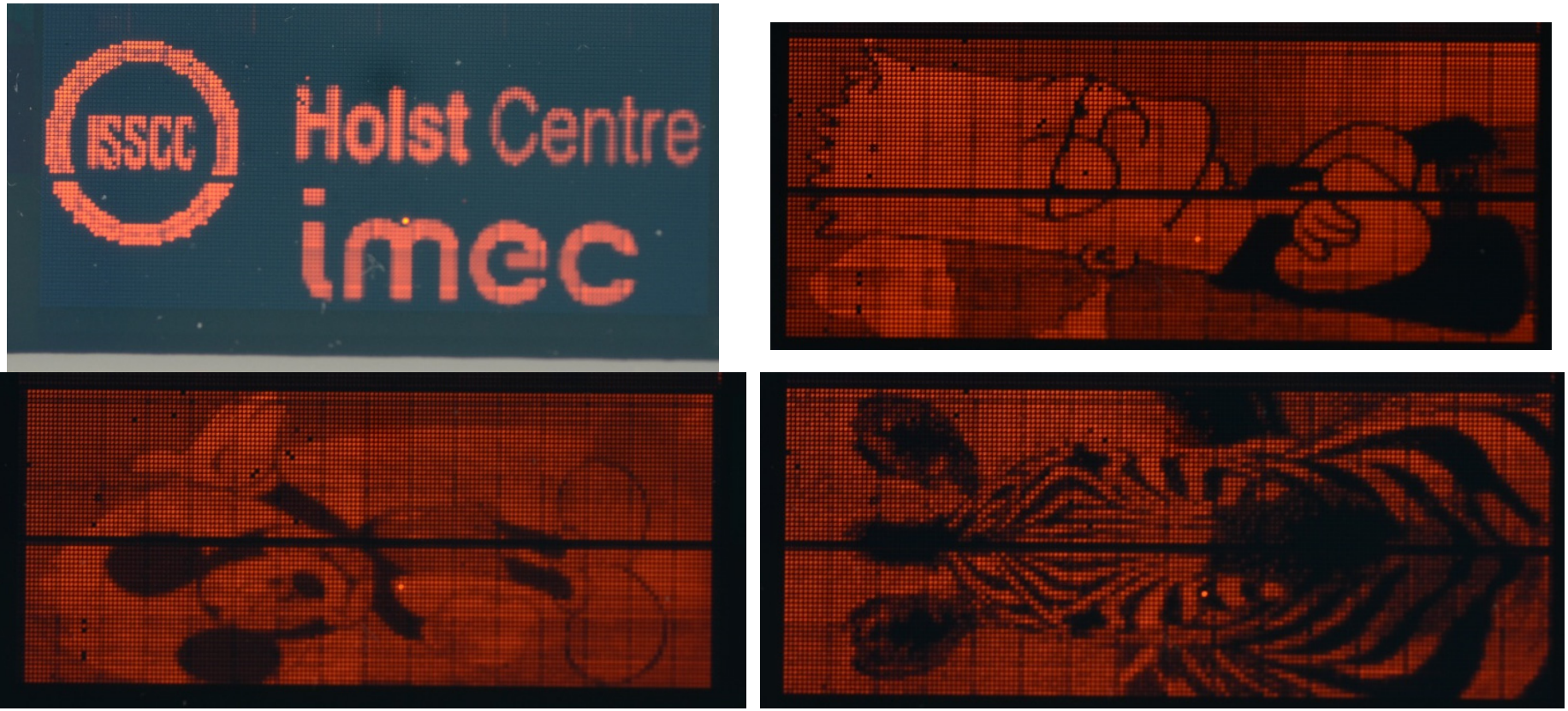
Experimental display for digital driving testing
Comprising an integrated line driver

6 inch foil

Classical AMOLED display

2 individual line drivers for design testing

Images



Conclusion

- A dedicated line driver in an a-IGZO technology on foil has been designed and tested that enables
  - Pulse Width Modulation (PWM) of pixels in AMOLED displays
  - Clocking speeds up to 360 kHz @ 11V V_{DD}
- Substantial reduction of the AMOLED display power consumption is obtained.
  - Currently shown 38%
  - Future embodiments >50%

Acknowledgements

This work was performed in collaboration between IMEC and TNO in the frame of the HOLST Centre

Organic-Transistor-Based 2kV ESD-Tolerant Flexible Wet Sensor Sheet for Biomedical Applications with Wireless Power and Data Transmission Using 13.56MHz Magnetic Resonance

H. Fuketa[1,2], K. Yoshioka[1,2], T. Yokota[1,2], W. Yukita[1,2], M. Koizumi[1,2], M. Sekino[1,2], T. Sekitani[1,2], M. Takamiya[1,2], T. Someya[1,2], and T. Sakurai[1,2]

[1]The University of Tokyo
[2]JST/ERATO

Outline

- Background
- Flexible wet sensor sheet with organic transistor circuit
  - Wet sensor based on organic RC oscillator
  - Adaptive amplitude control (AAC)
  - ESD protection with organic Schottky diodes
- Conclusion

Outline

- Background
- Flexible wet sensor sheet with organic transistor circuit
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- Conclusion

Background

Wet sensor for biomedical, nursing-care, elder-care applications

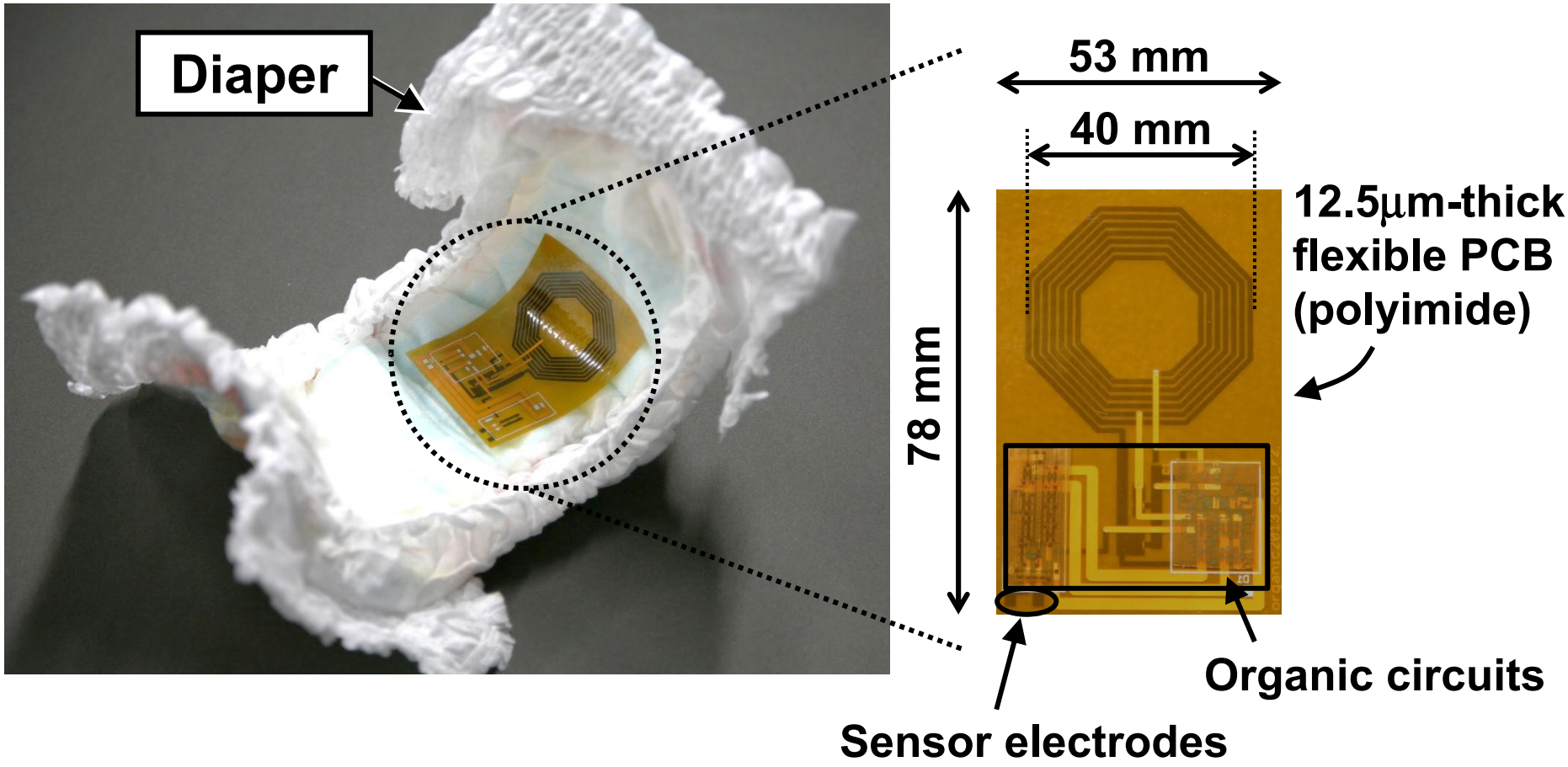
Requirements

- ✓ Thin and mechanically flexible
- ✓ Wireless power and data transmission
- ✓ Low-cost (disposable)

Detection of urination in diapers

Flexible wet sensor sheet (1/2)

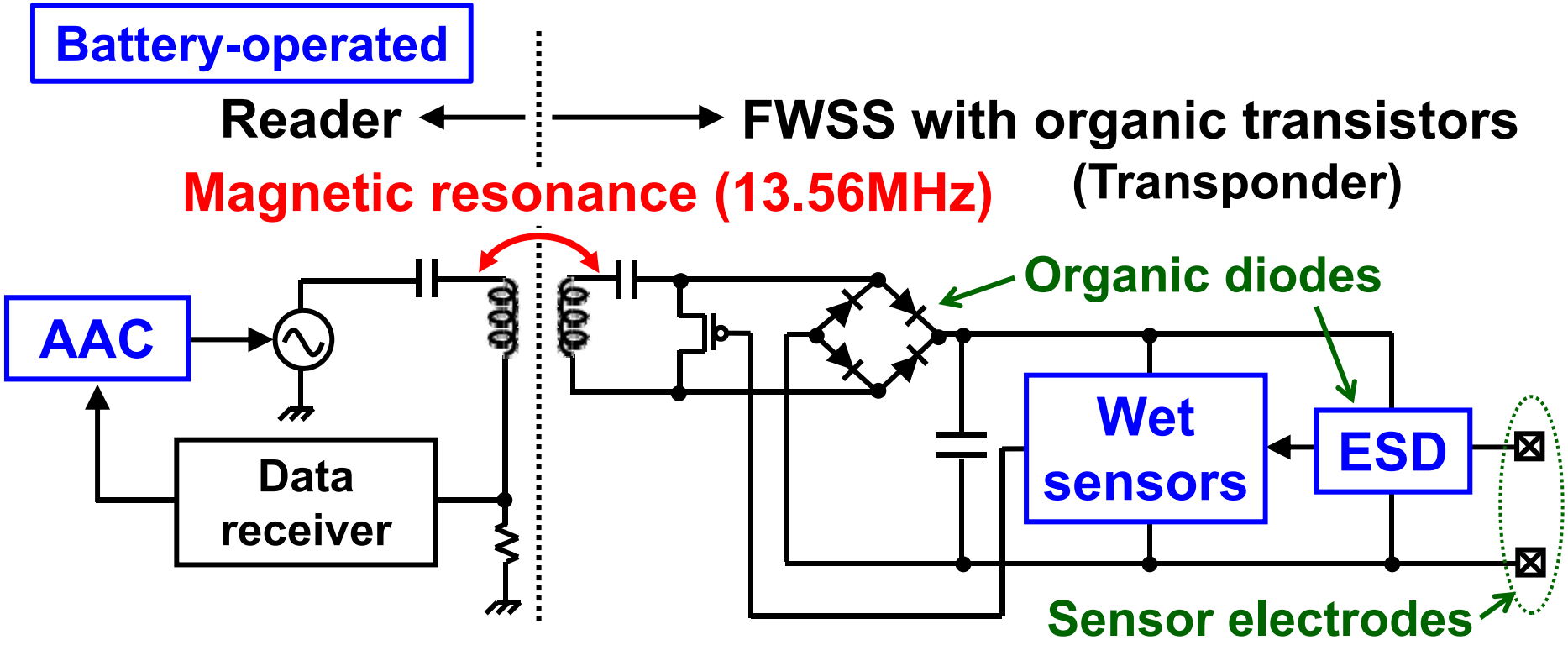
Flexible wet sensor sheet (FWSS) for urination detection with organic transistors



Flexible wet sensor sheet (2/2)

Features of developed FWSS:

- Wet sensor based on organic RC oscillator
- Adaptive amplitude control (AAC)
- ESD protection circuit with organic Schottky diodes



Outline

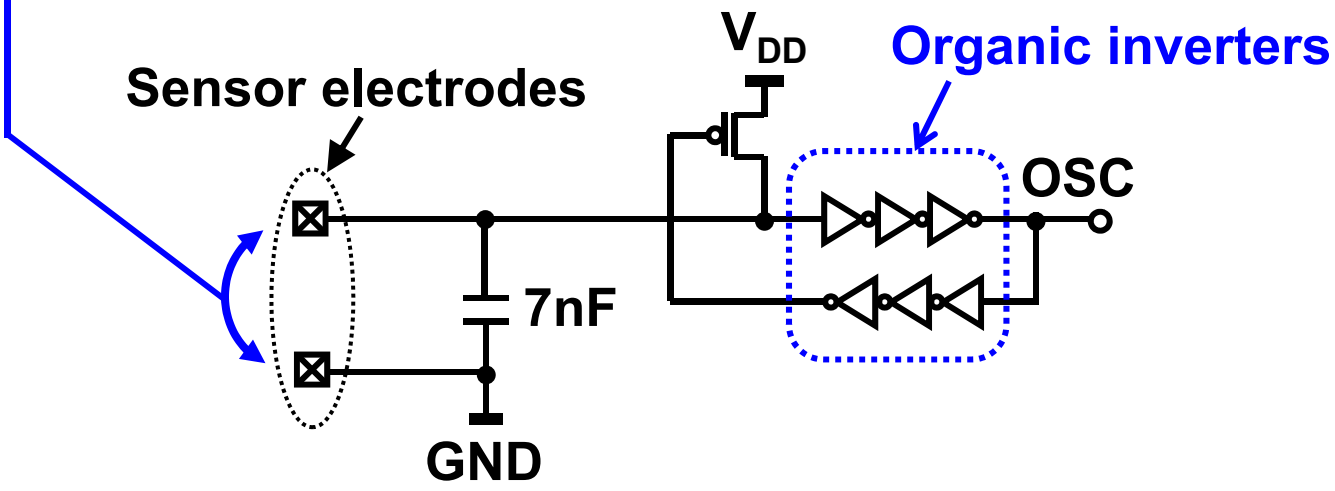
- Background
- **Flexible wet sensor sheet with organic transistor circuit**
  - **Wet sensor based on organic RC oscillator**
  - **Adaptive amplitude control (AAC)**
  - **ESD protection with organic Schottky diodes**
- Conclusion

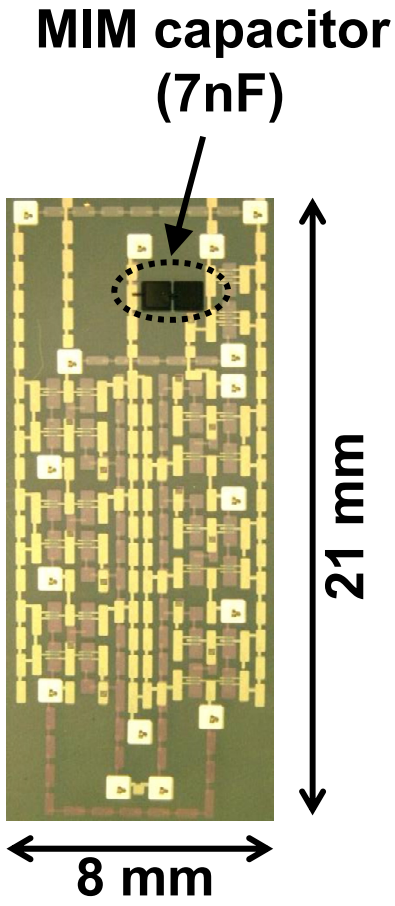
Organic wet sensor (1/2)

RC oscillator with organic pseudo-CMOS* inverters

Oscillation frequency depends on resistance between sensor electrodes (R_S).

- Dry (no urination) : $R_S \rightarrow \infty$ (No oscillation)
- Wet (urination) : R_S ~ several mega-ohms (normal saline)

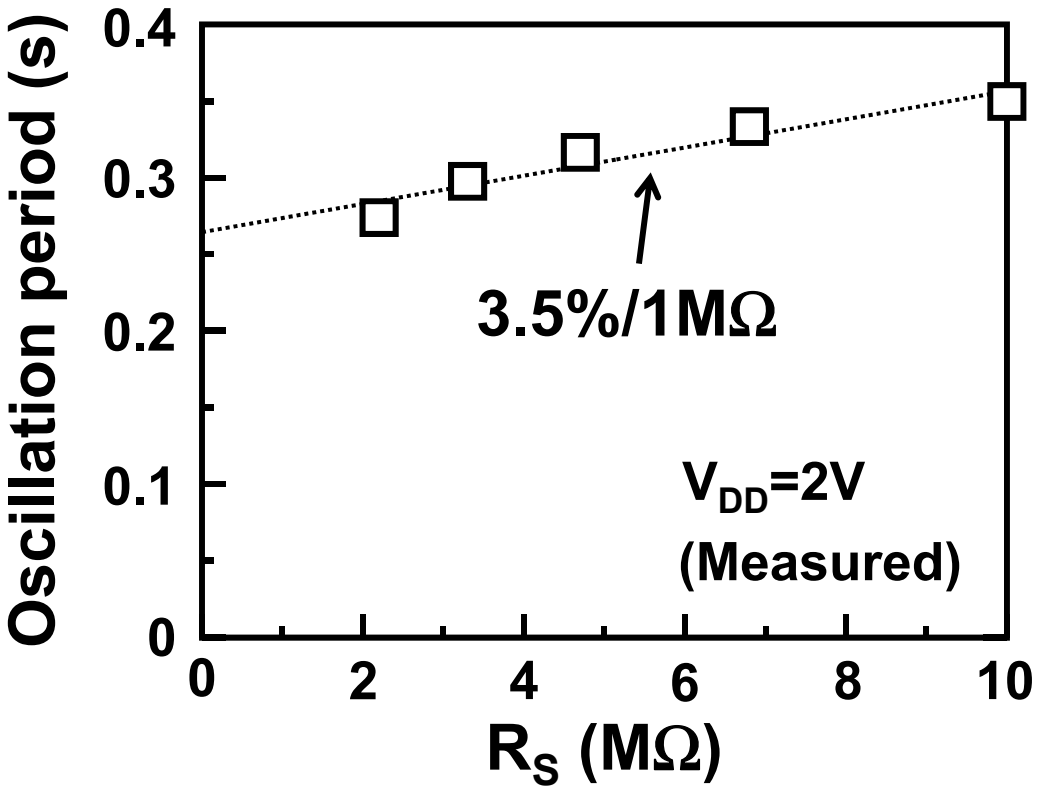




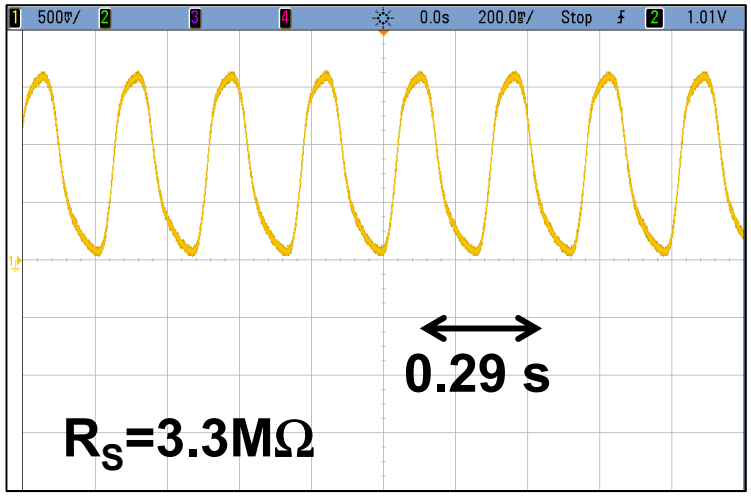
* T.-C. Huang, et al., DATE 2010.

Organic wet sensor (2/2)

Resistance dependence of oscillation period



Measured waveform



- Oscillation period is proportional to R_S.
- Power dissipation: 1.4μW @ 3Hz

Wireless power transmission

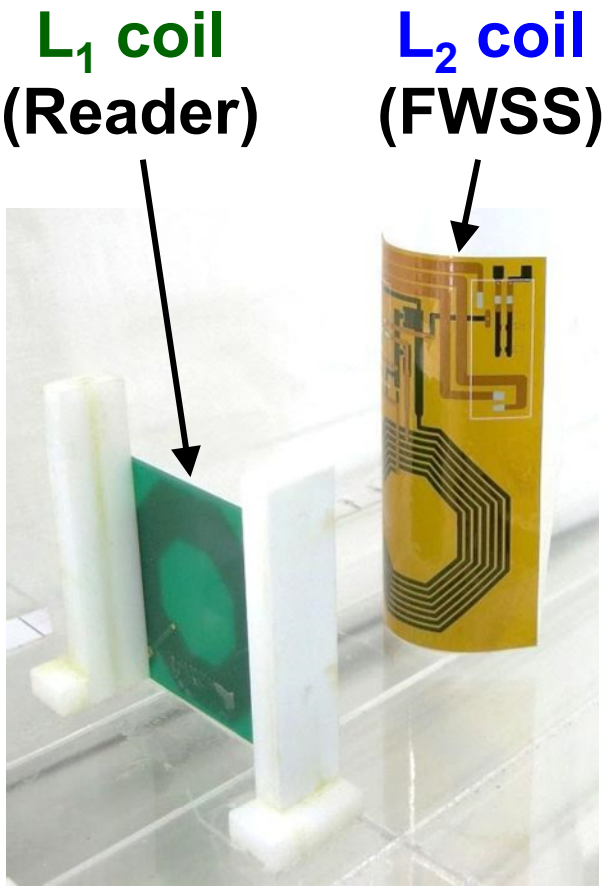
Power transmission efficiency degrades due to:

- **Increase in distance between reader coil (L_1) and FWSS coil (L_2)**
- **Bend of flexible FWSS coil (L_2)**

Reader must transmit maximum power to deal with degradation.

Power consumption of reader increases.

→ Problem in battery-operated reader



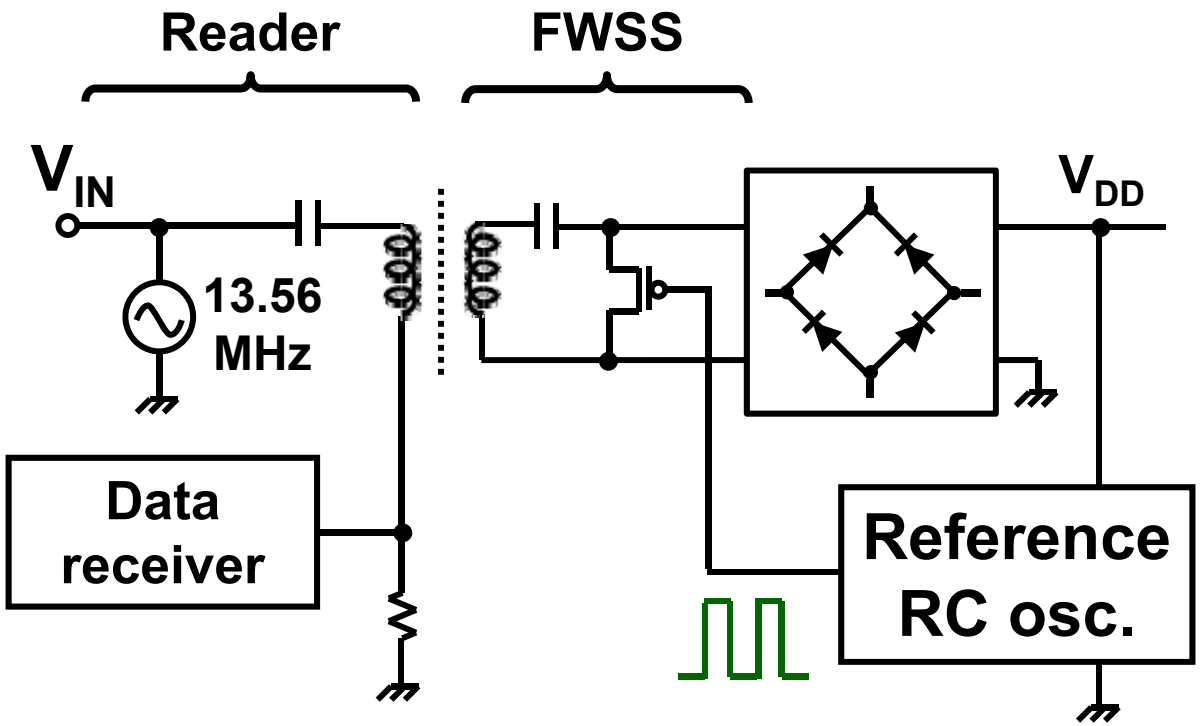
Adaptive amplitude control (1/2)

Amplitude of transmitted signal is adaptively controlled.

- **Oscillation of reference RC oscillator is monitored.**

  No oscillation → Amplitude V_{IN} increases.

➔ Minimum V_{IN} for correct operation of FWSS is tracked.



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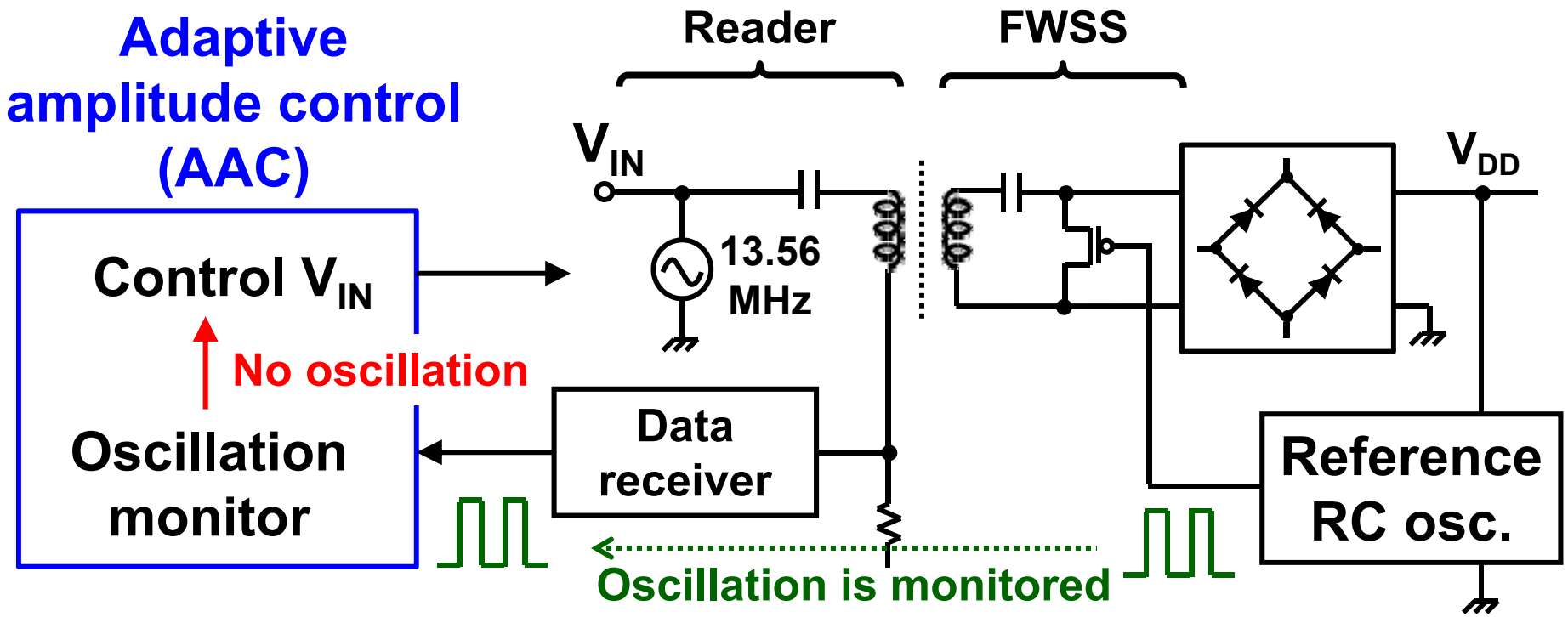
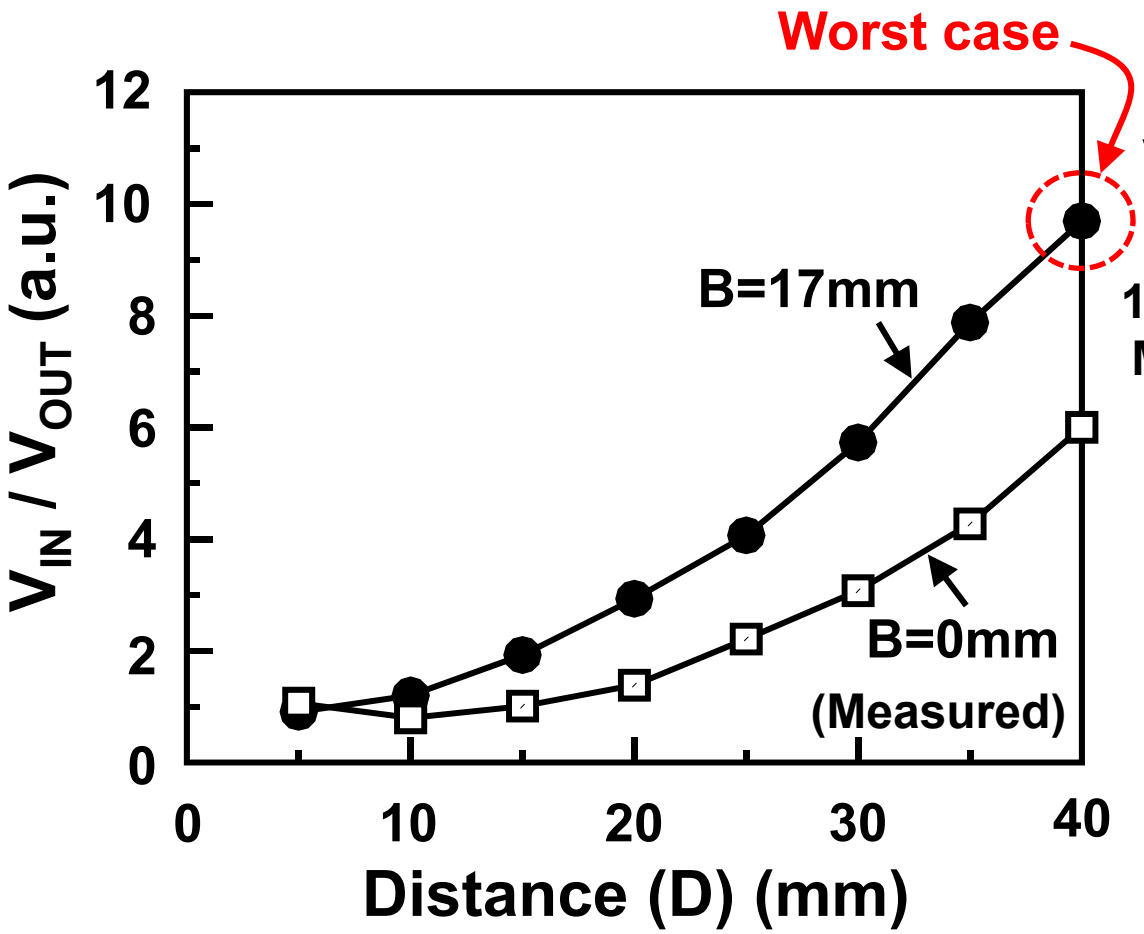
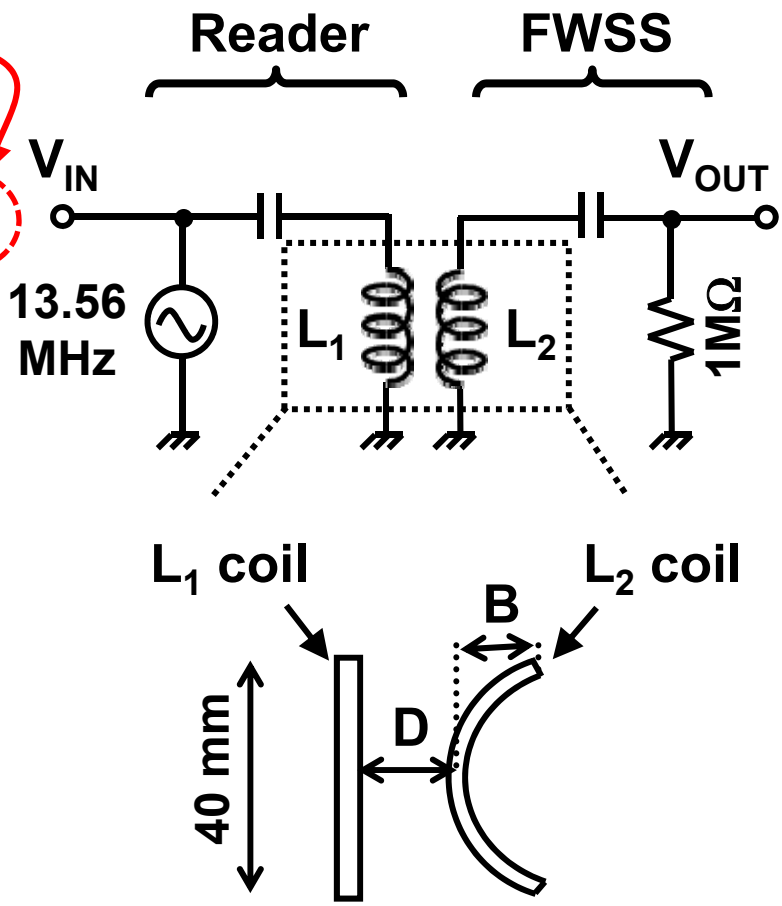
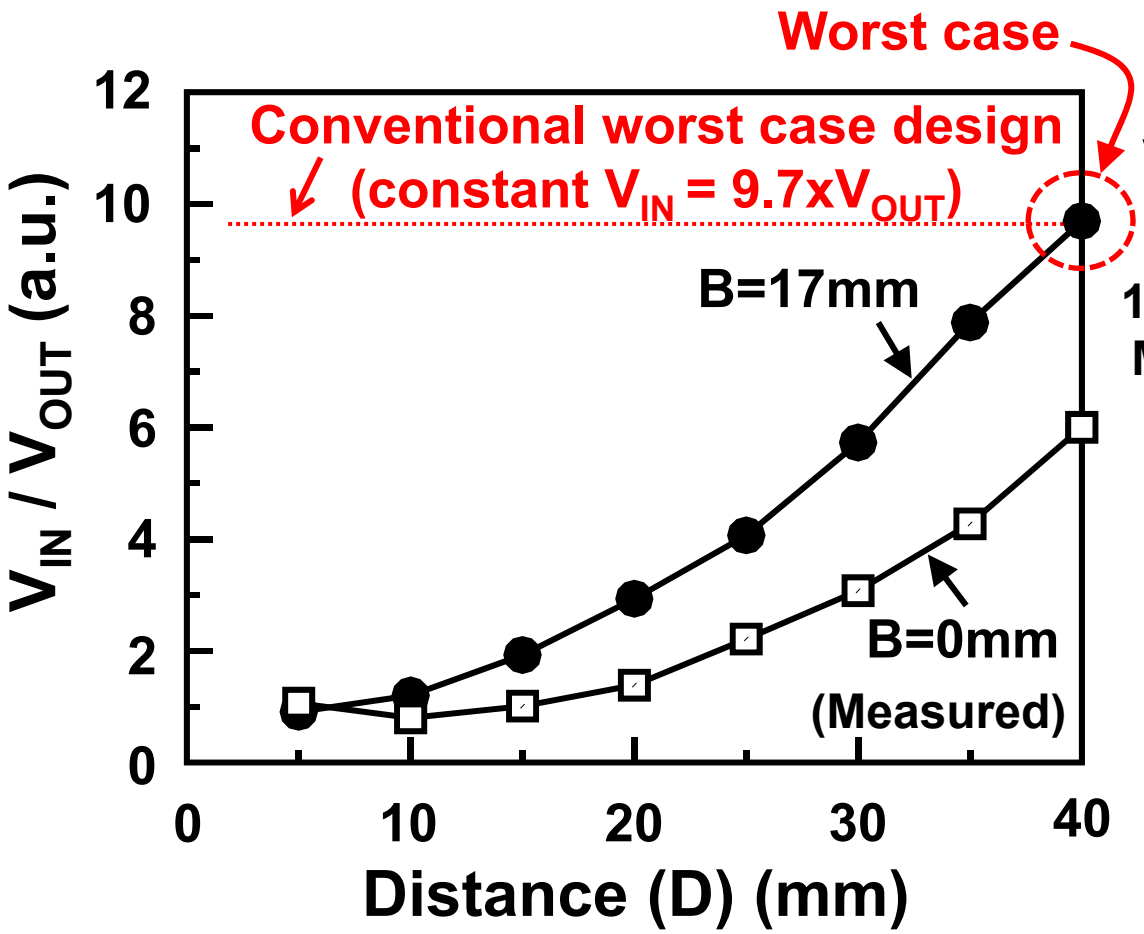


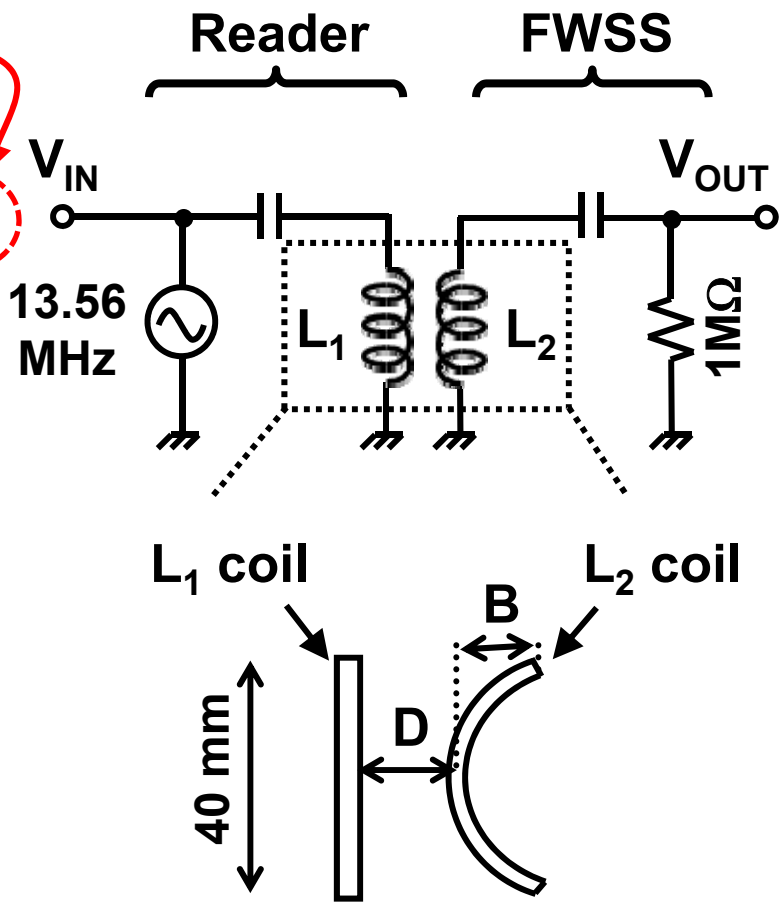
Adaptive amplitude control (2/2)



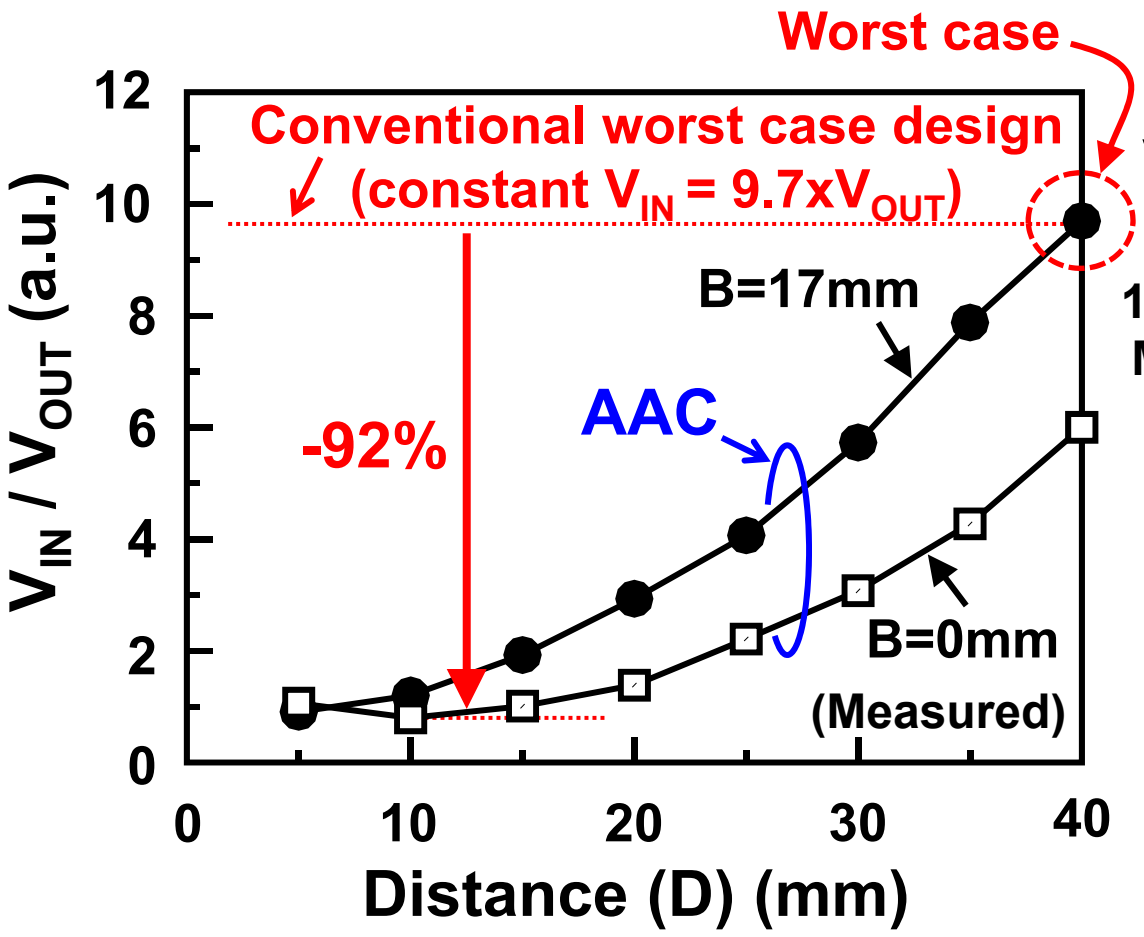


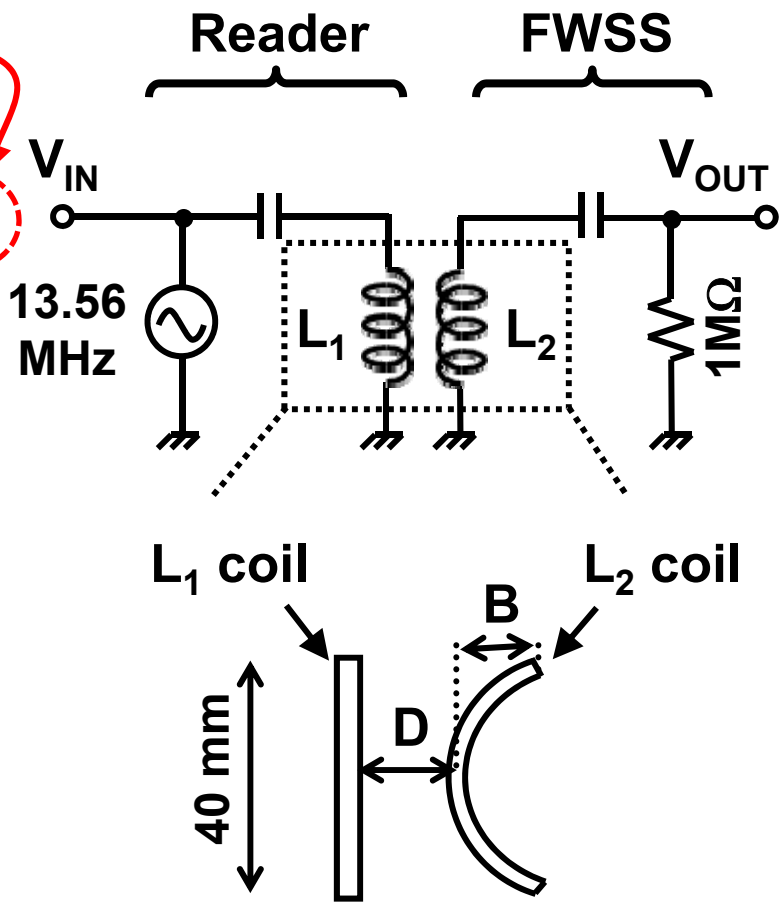
Adaptive amplitude control (2/2)





Adaptive amplitude control (2/2)





AAC reduces amplitude up to 92% compared with conventional worst case design.

ESD protection

Sensor electrodes could contact with a wet human skin.

➔ ESD protection is imperative in FWSS.

ESD protection has not been taken into account for organic circuits.

Goal of this paper

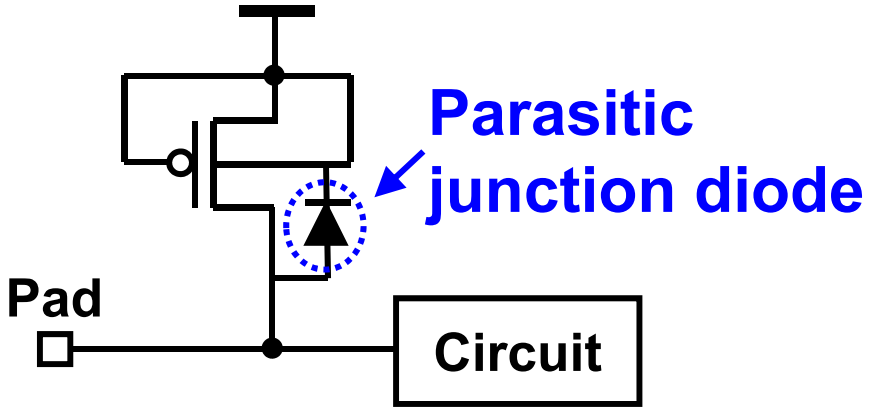
- **ESD protection circuit is investigated for organic circuits.**
- **ESD tolerance is checked according to ESD standard of IEC 61000-4-2.**

Problem of ESD in organic transistors

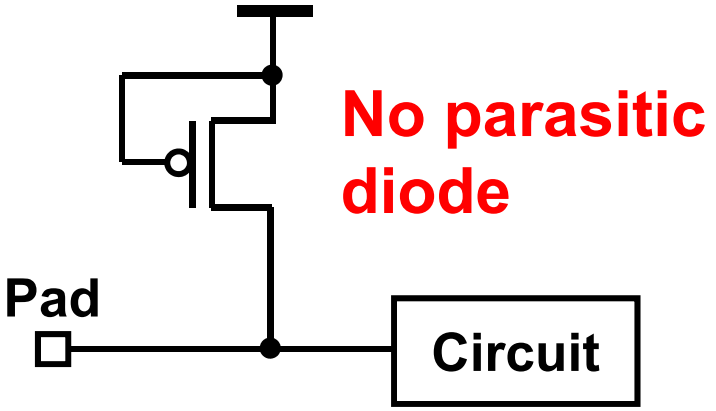
Organic transistors are fabricated on insulating film.

➔ ESD protection in organic transistors is difficult.

ESD in Si transistors



ESD in organic transistors



ESD protection with organic diodes (1/2)

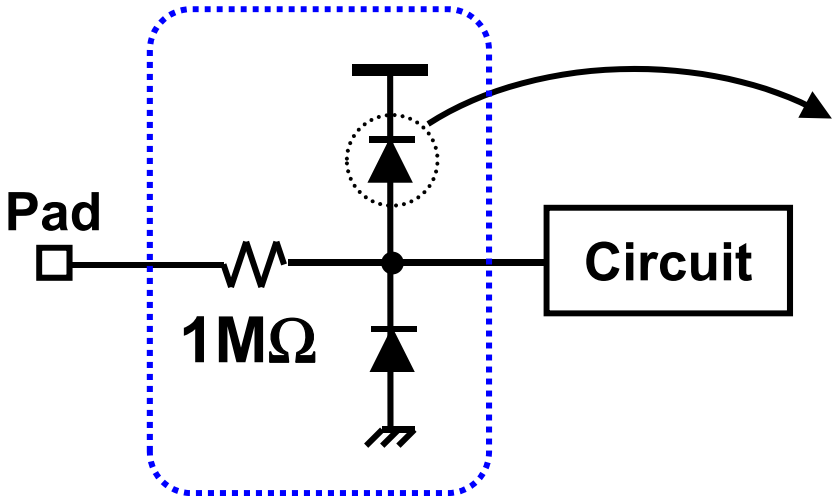
Schottky diode with copper phthalocyanine (CuPc)

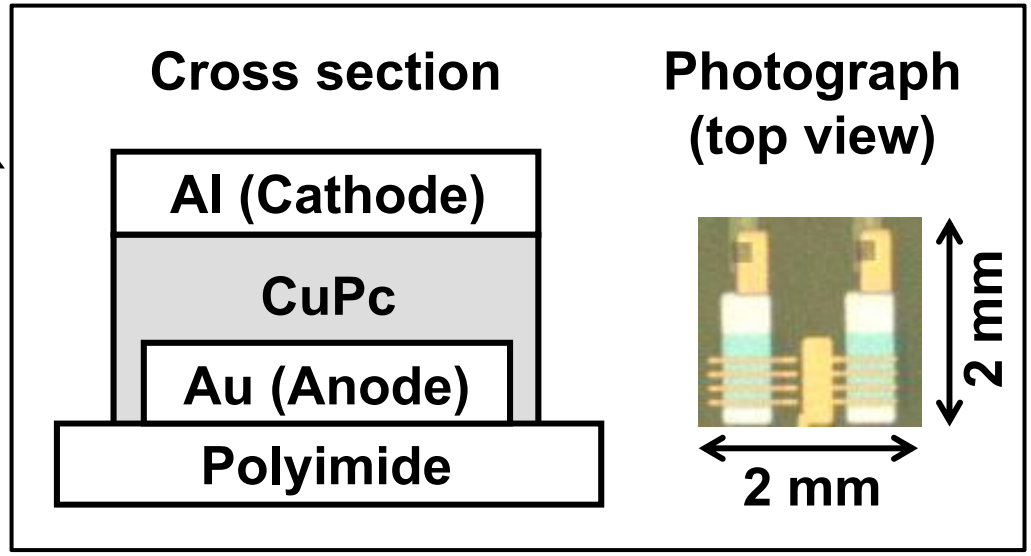
- Vertical structure [4]

  → - Larger current drivability
    - Better frequency characteristic
    (→ Also used for rectifier)

[4] Y. Ai, et al., Appl. Phys. Lett. 90, 262105 (2007).

ESD protection circuit with organic diode



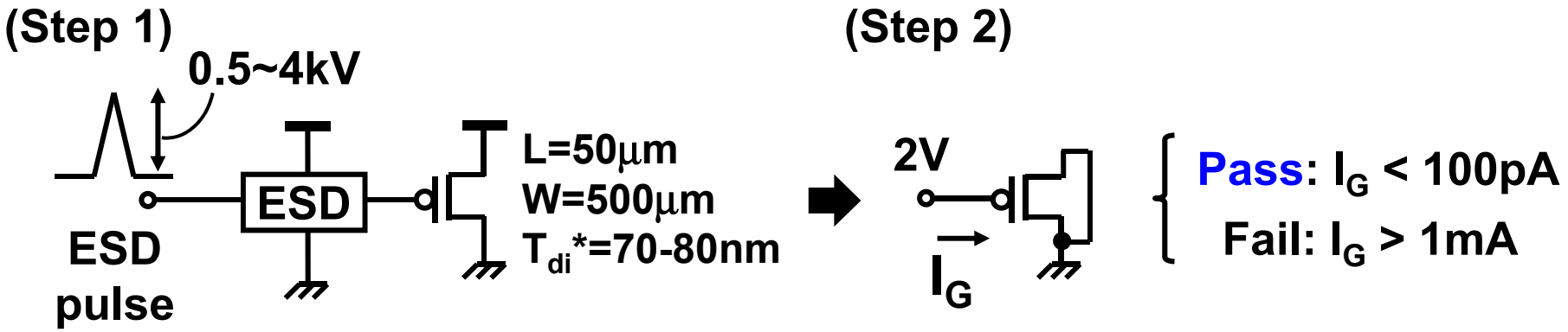


ESD protection with organic diodes (2/2)

ESD measurement (IEC 61000-4-2)

- ESD tolerance is checked by measuring gate current.

➔ 2kV ESD tolerance is achieved.



	Initial	0.5kV	1kV	2kV	4kV
Without ESD Protection	Pass	Fail	Fail	Fail	Fail
With ESD Protection	Pass	Pass	Pass	Pass	Fail

(*) T_{di}: Thickness of gate dielectric (parylene)

Conclusion

- **Flexible wet sensor sheet (FWSS) for urination detection with organic transistors**
  - **Adaptive amplitude control (AAC)**
    - ➔ **AAC deals with bend of flexible coil for the wireless power transmission and reduces amplitude up to 92%.**
    - ➔ **Power consumption of reader can be reduced.**
  - **ESD protection with organic diode**
    - ➔ **2kV ESD tolerance is achieved.**

Both AAC and ESD are essential in the wireless and flexible sensors for biomedical applications.

A 13.56MHz RFID Tag with Active Envelope Detection in an Organic Complementary TFT Technology

Vincenzo Fiore[1],
E. Ragonese[2], S. Abdinia[3], S. Jacob[4],
I. Chartier[4], R. Coppard[4], A. van Roermund[3],
E. Cantatore[3], G. Palmisano[1]

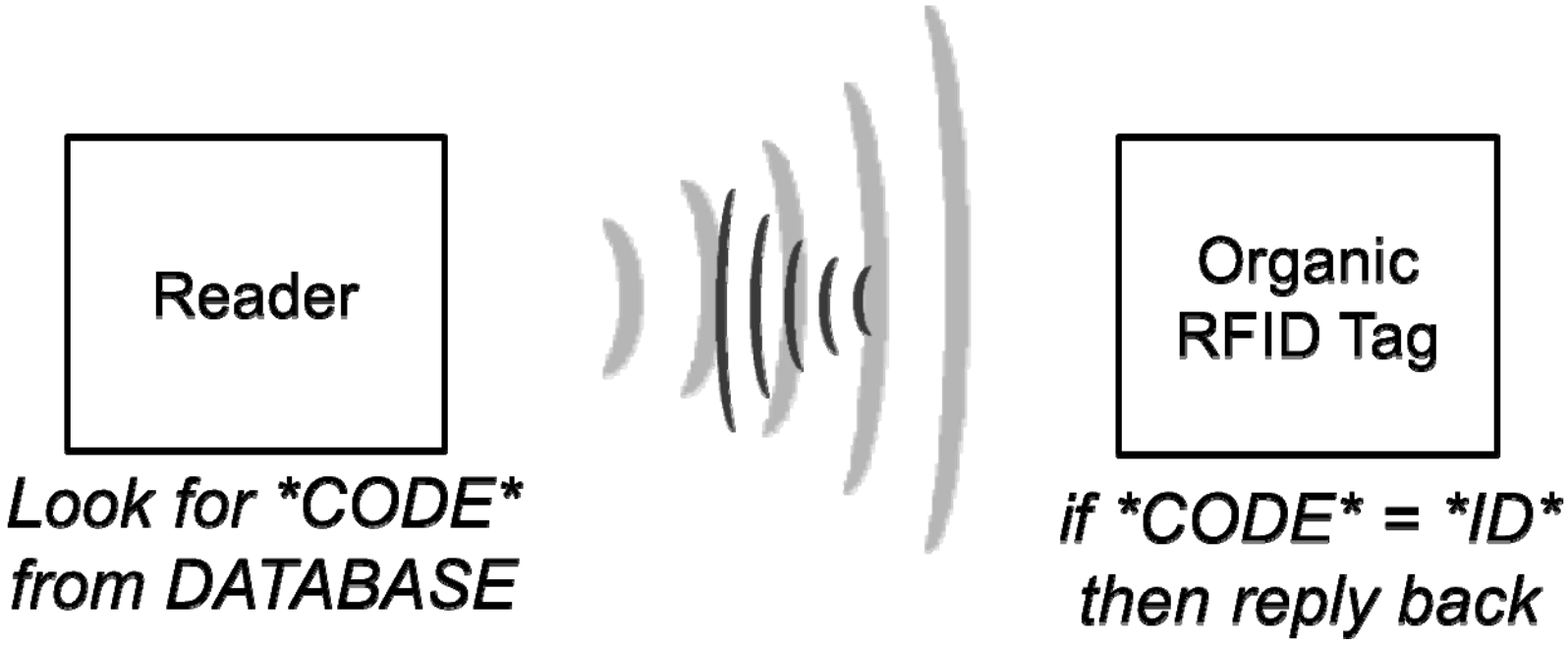
[1]University of Catania, Catania, Italy, [2]STMicroelectronics, Catania, Italy,
[3]Eindhoven University of Technology, Eindhoven, The Netherlands,
[4]CEA-LITEN, Grenoble, France

Introduction:
toward organic RFID tags

Myny,	ISSCC'08	without RX, p-type TFTs
Blache,	ISSCC'09	without RX, complementary-OTFTs
Myny,	ISSCC'12	OOK RX, hybrid organic/metal-oxide
=>	*ISSCC'14*	*ASK RX, printed complementary-OTFT*

Introduction: *"Silent Tag"*

Typical issues are security and identification.



Patented identification scheme:

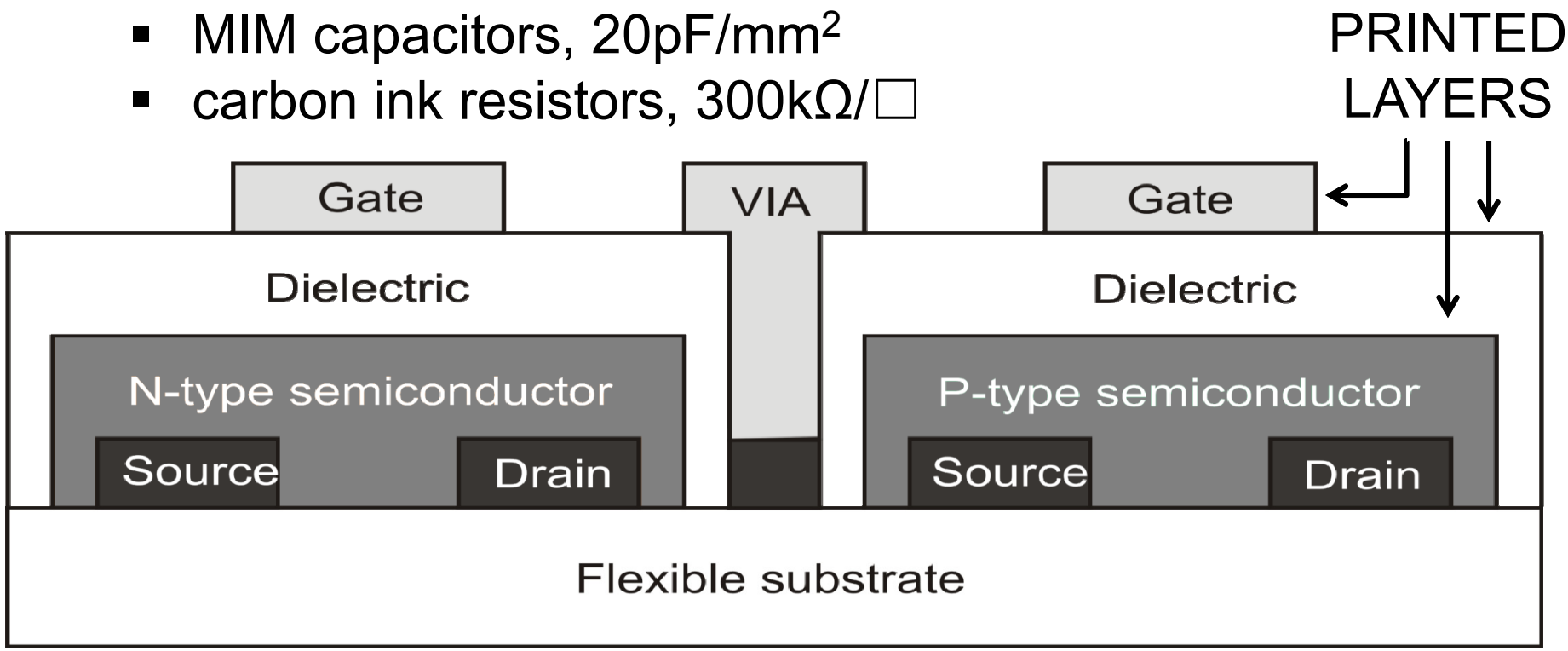
To have a search, a list of tags *must be known in advance*

- ✓ security provided without encryption
- ✓ enables effective tracking of tags

Technology

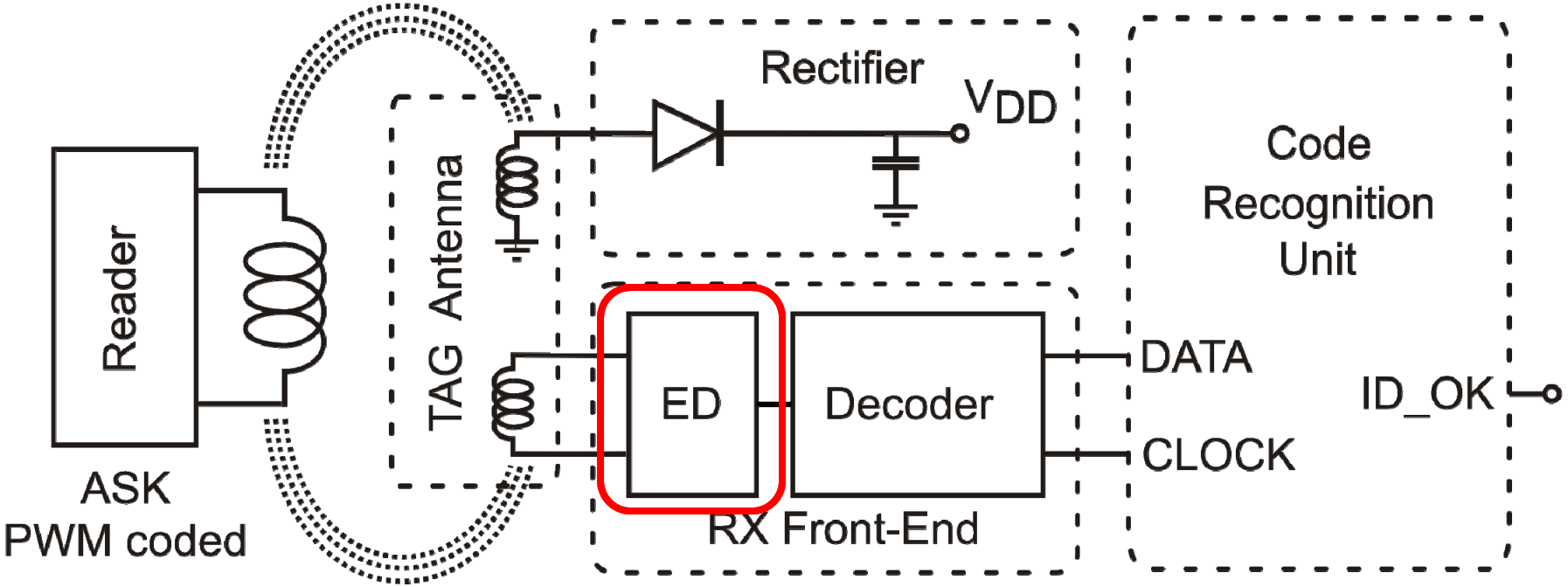
	μ_{SAT} [cm²/Vs]	$\lvert V_{T,SAT} \rvert$ [V]
n-type	0.55	18
p-type	1.50	20

- MIM capacitors, 20pF/mm²
- carbon ink resistors, 300kΩ/□



S. Jacob, et al, ESSDERC 2012

Architecture



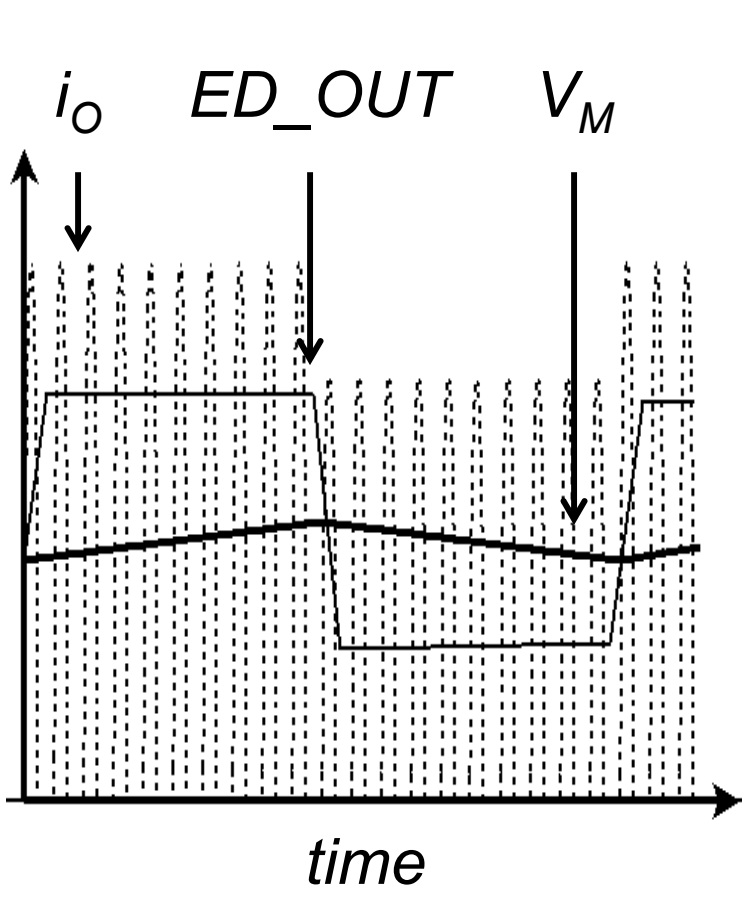
Two coils tag antenna

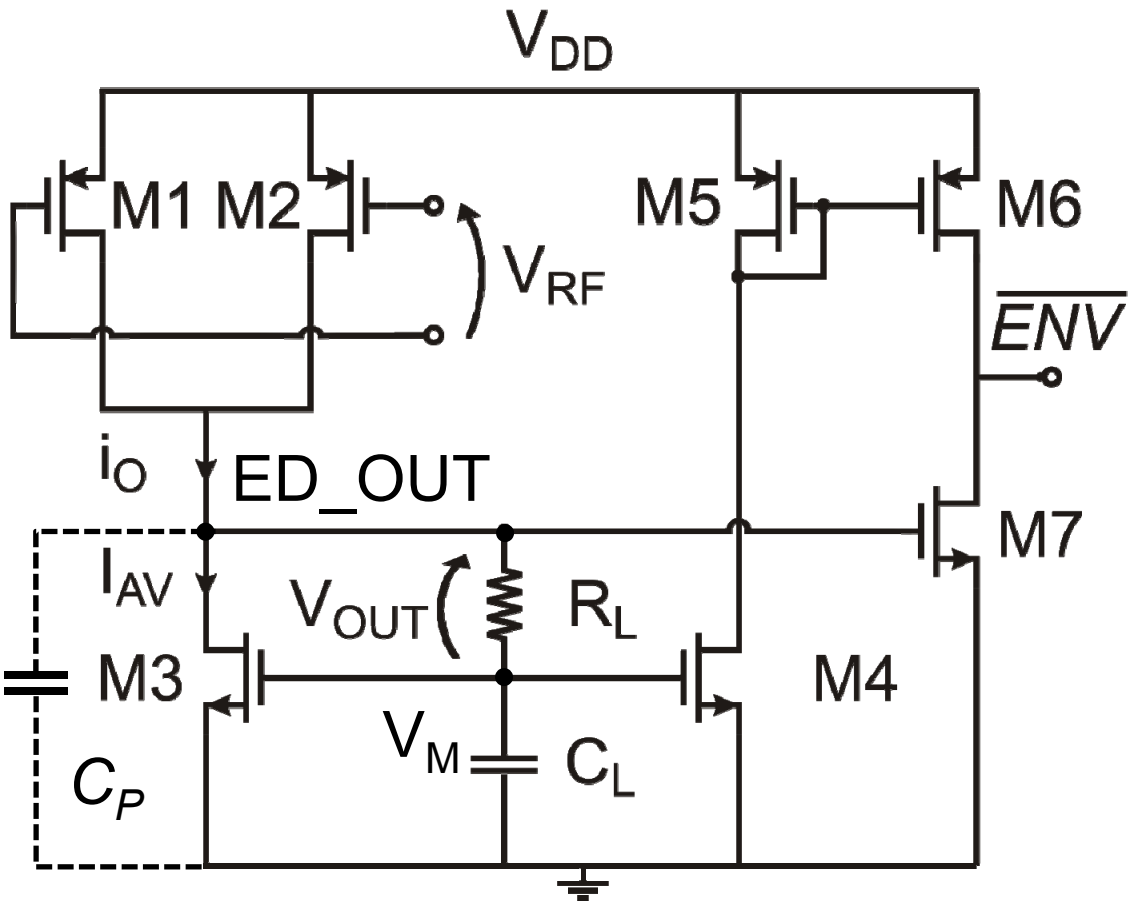
- ✓ enables higher input voltage at the rectifier

RX differential Front-End

- ✓ high input impedance, low power consumption

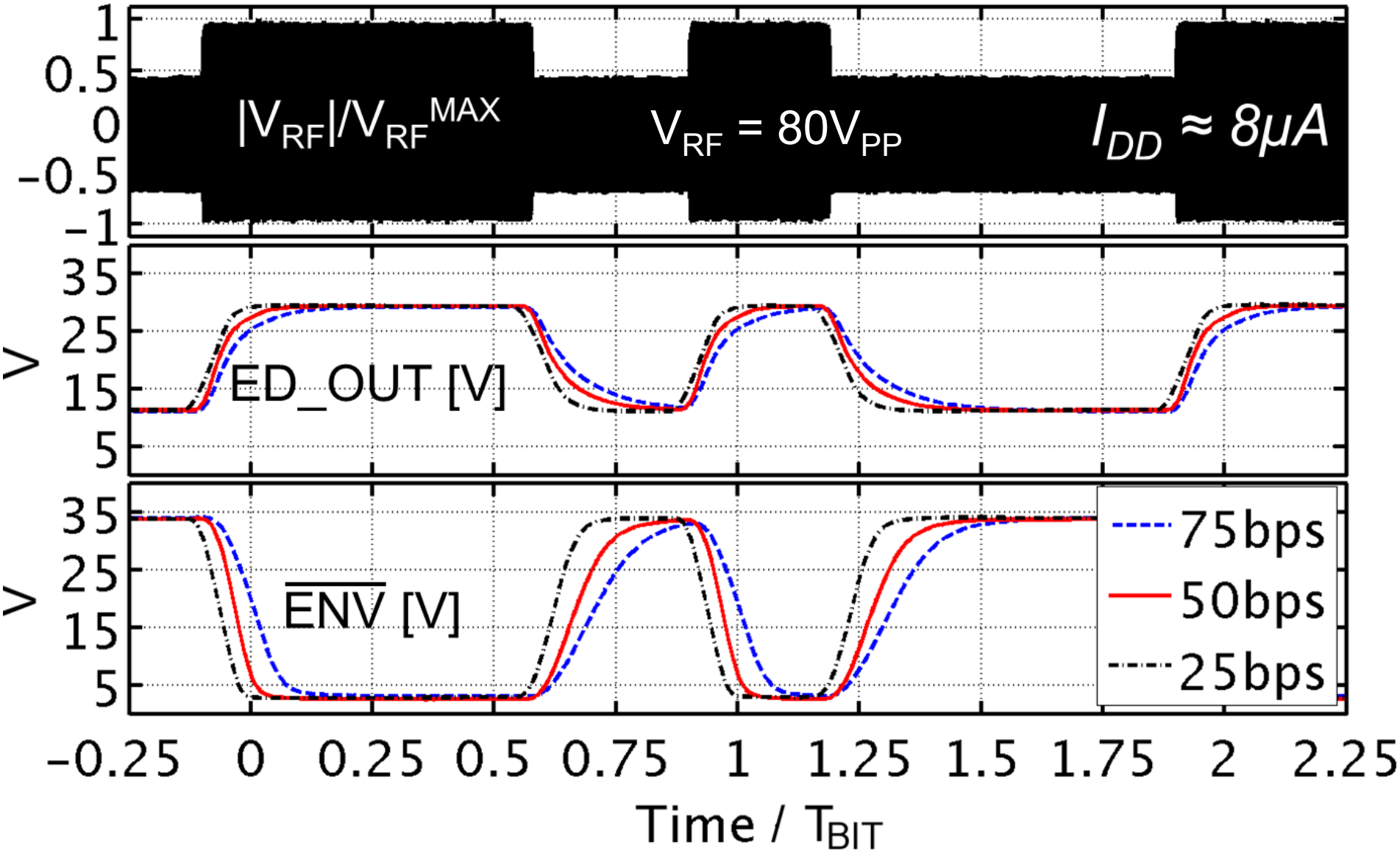
Receiver: ED design



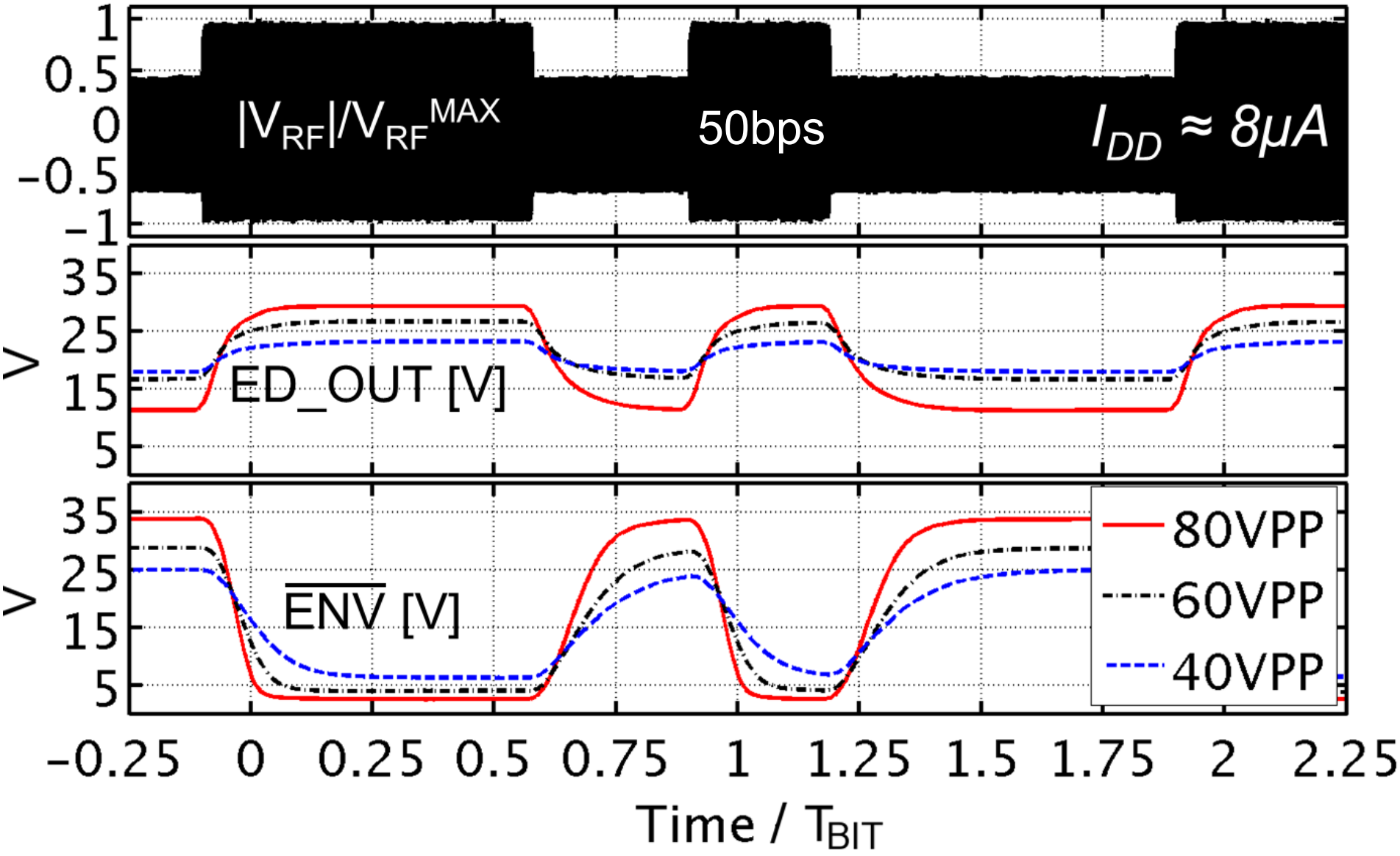


$$V_{OUT} \approx R_L \times \left(i_{O,AV} - I_{AV}\right) \quad R_L = 40M\Omega,\ C_L = 6nF$$

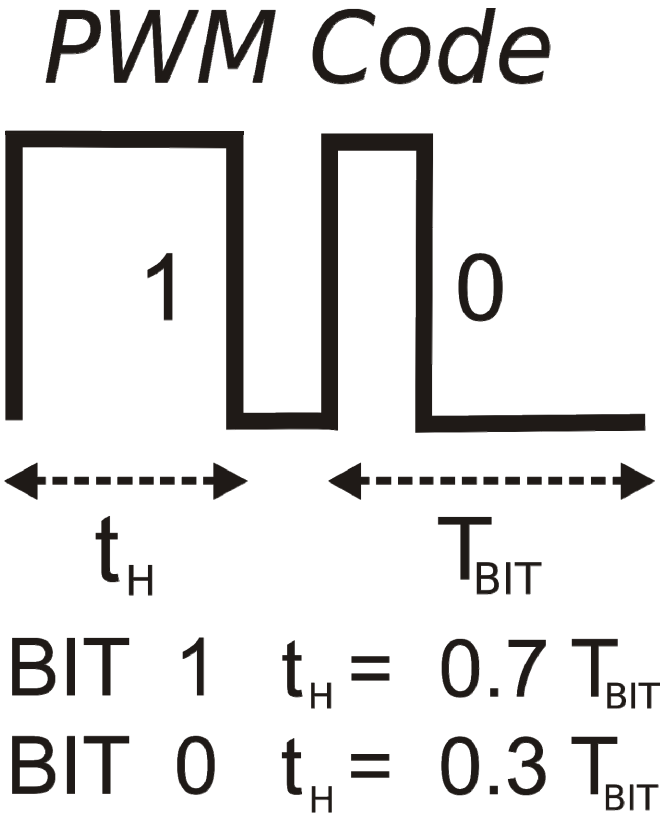
Receiver: ED measurements

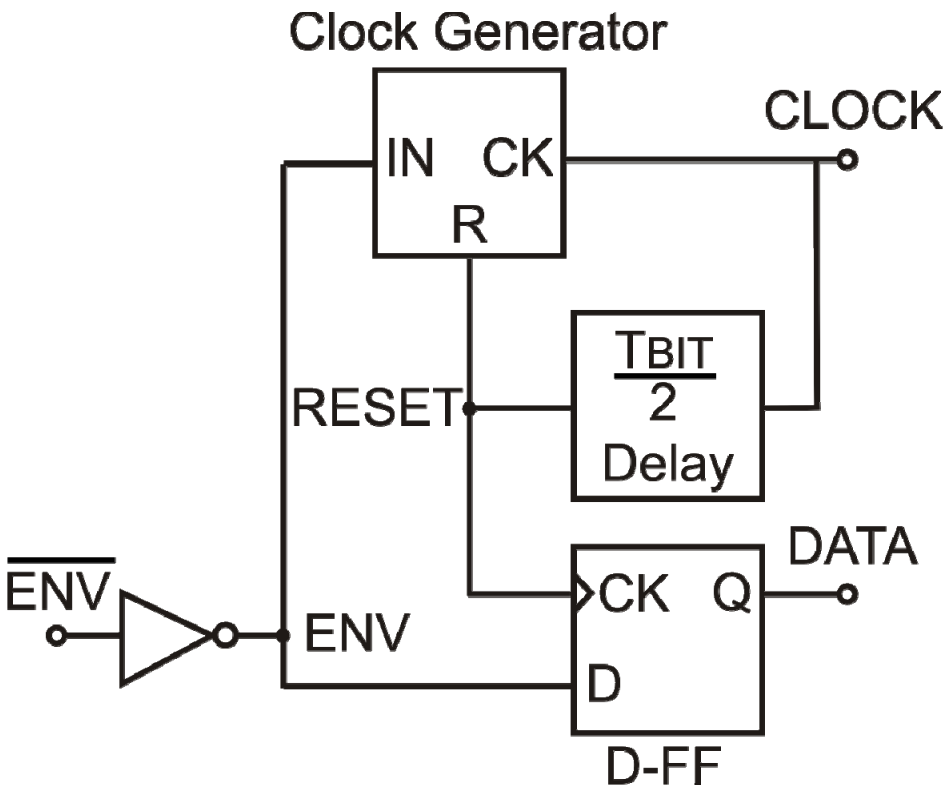


Receiver: ED measurements



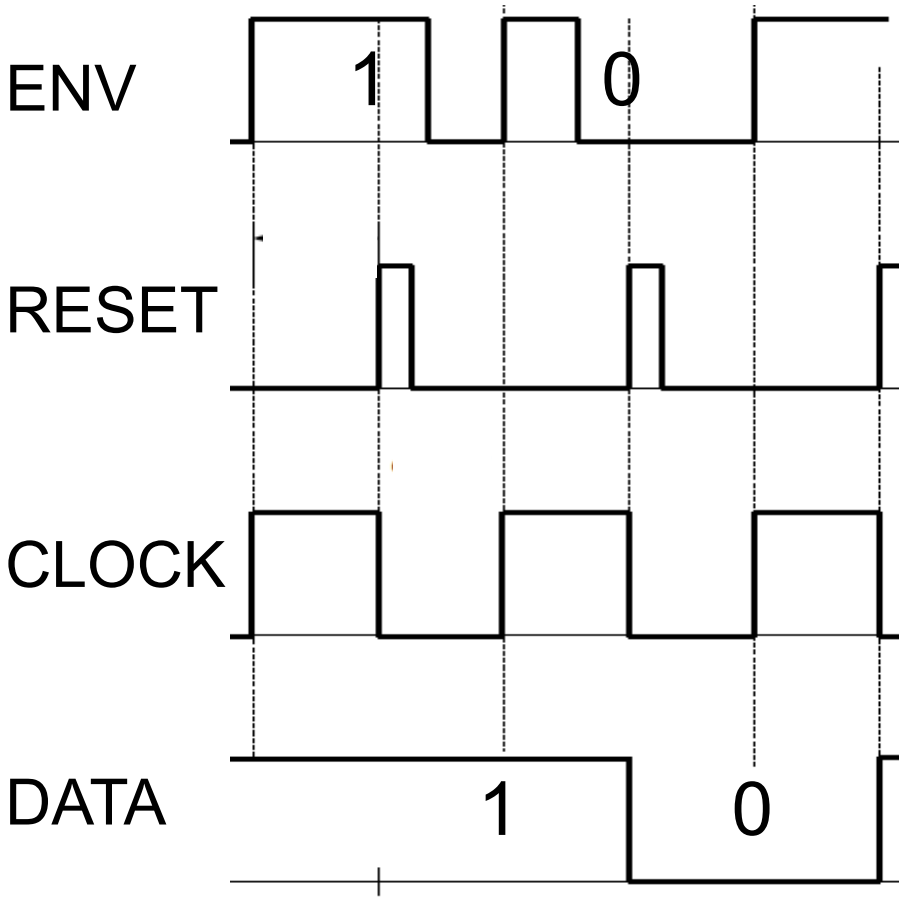
Receiver: Decoder design

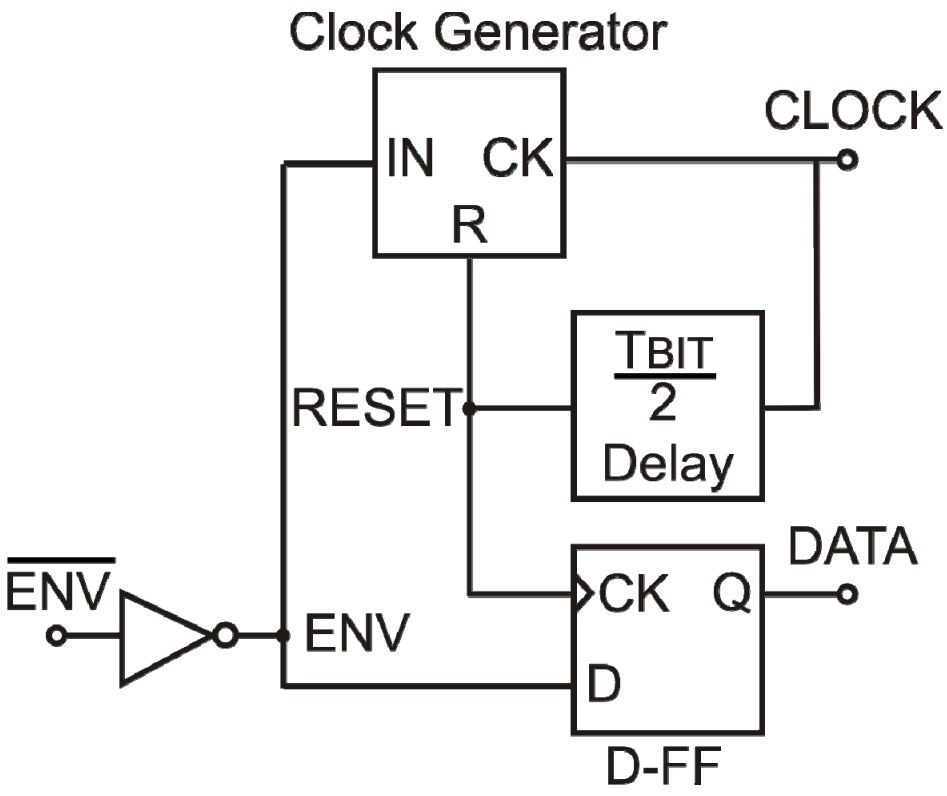




- PWM provides clock without complex circuitry
- Dynamic logic enables low power and transistor count

Receiver: Decoder design

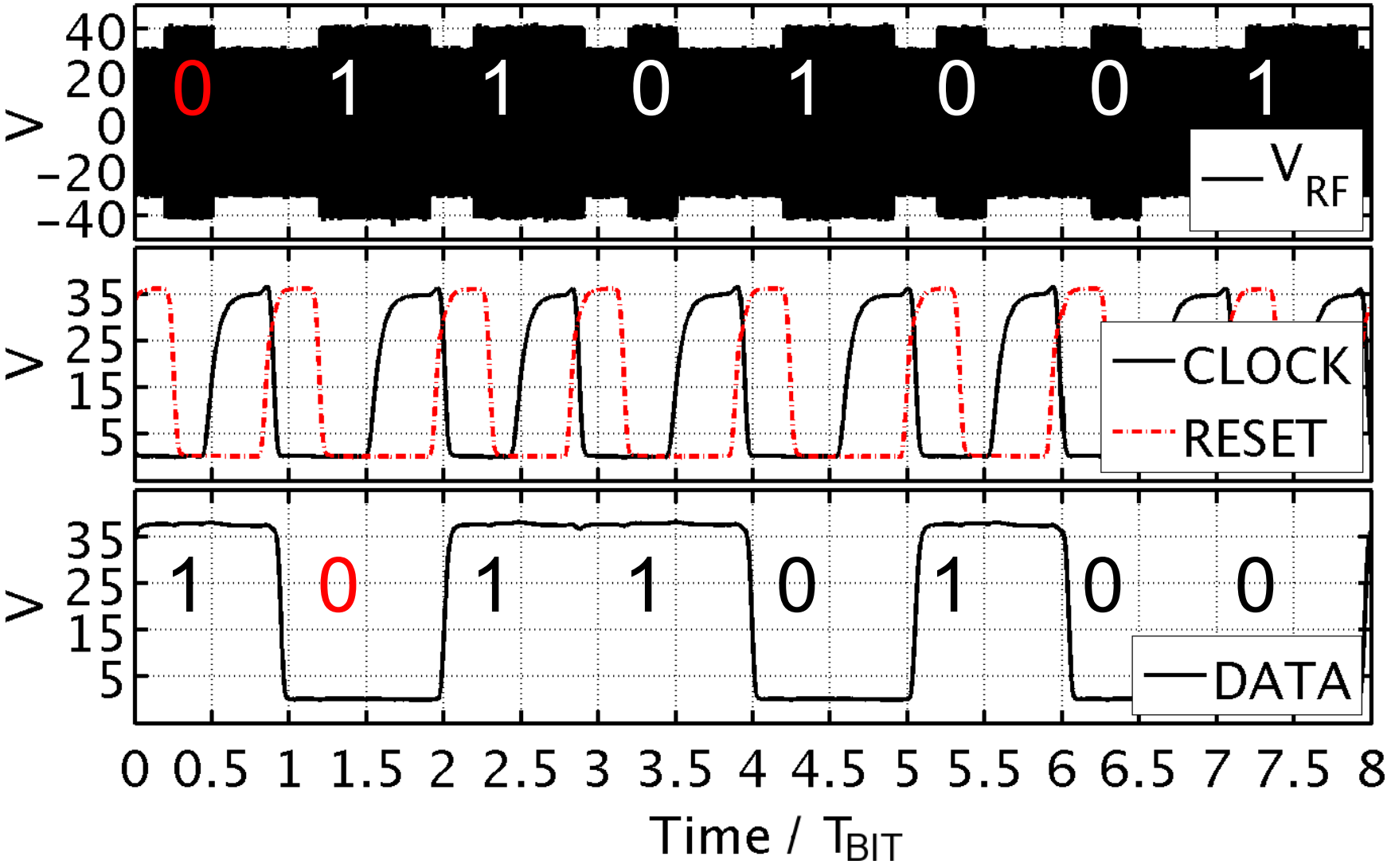




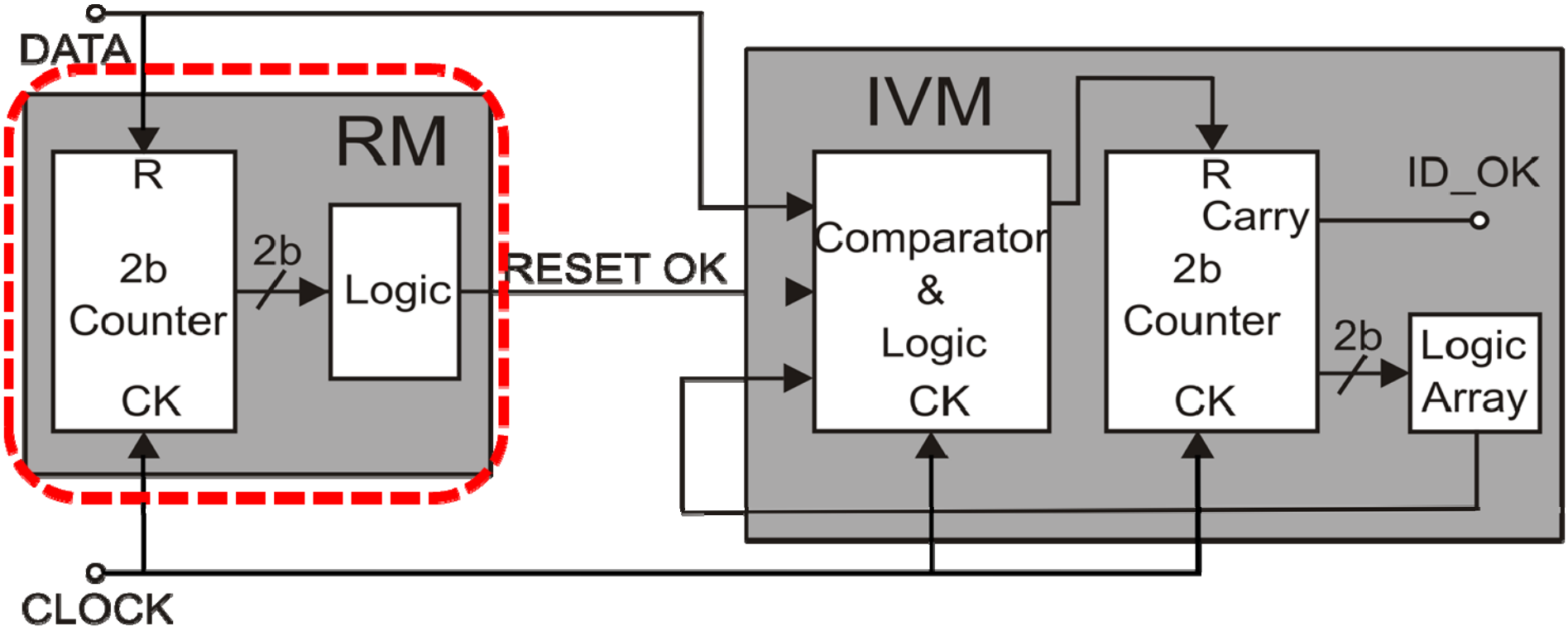
- Clock generator detects rising edges
- Asymmetric delay samples the input and reset

Receiver: measurements

25% ASK signal successfully received with a C-OTFT technology



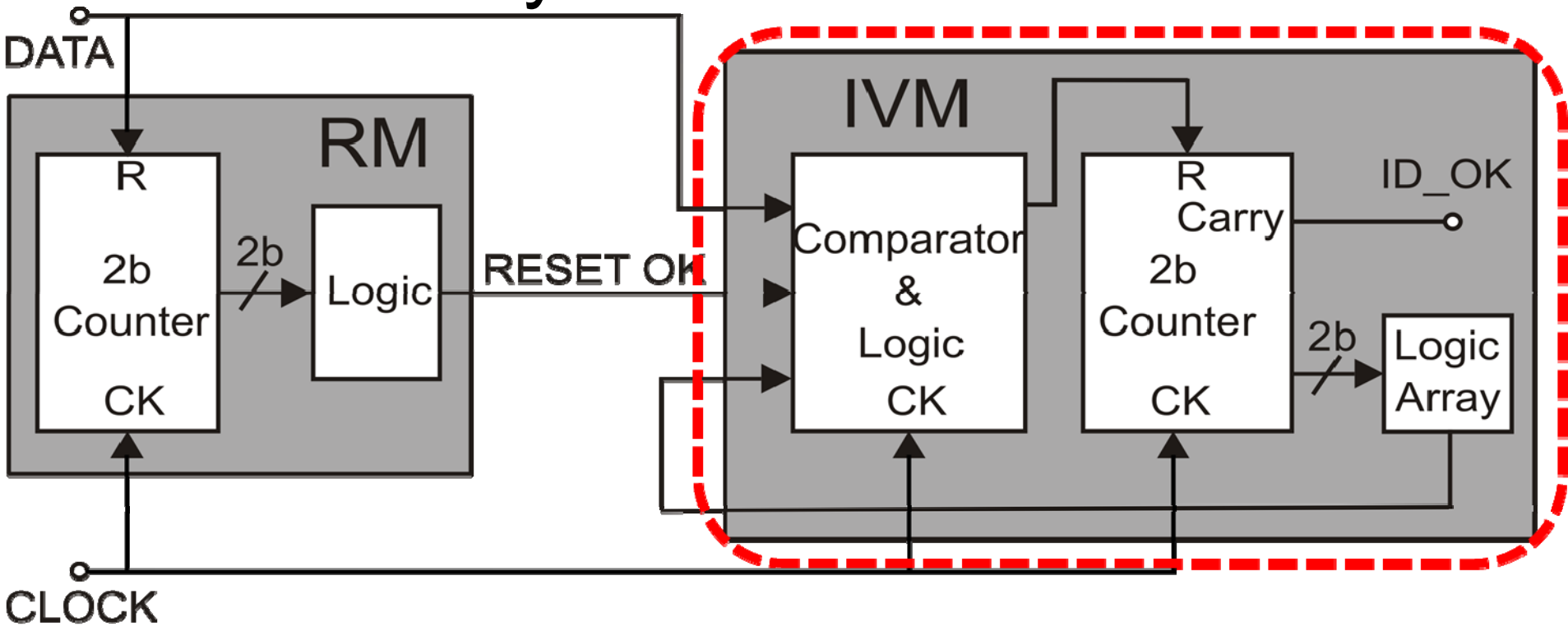
Code recognition unit: Reset Module



RM synchronizes the tag with the reader, announcing the arrival of a new code:

if DATA = "0000" then RESET OK = "1"

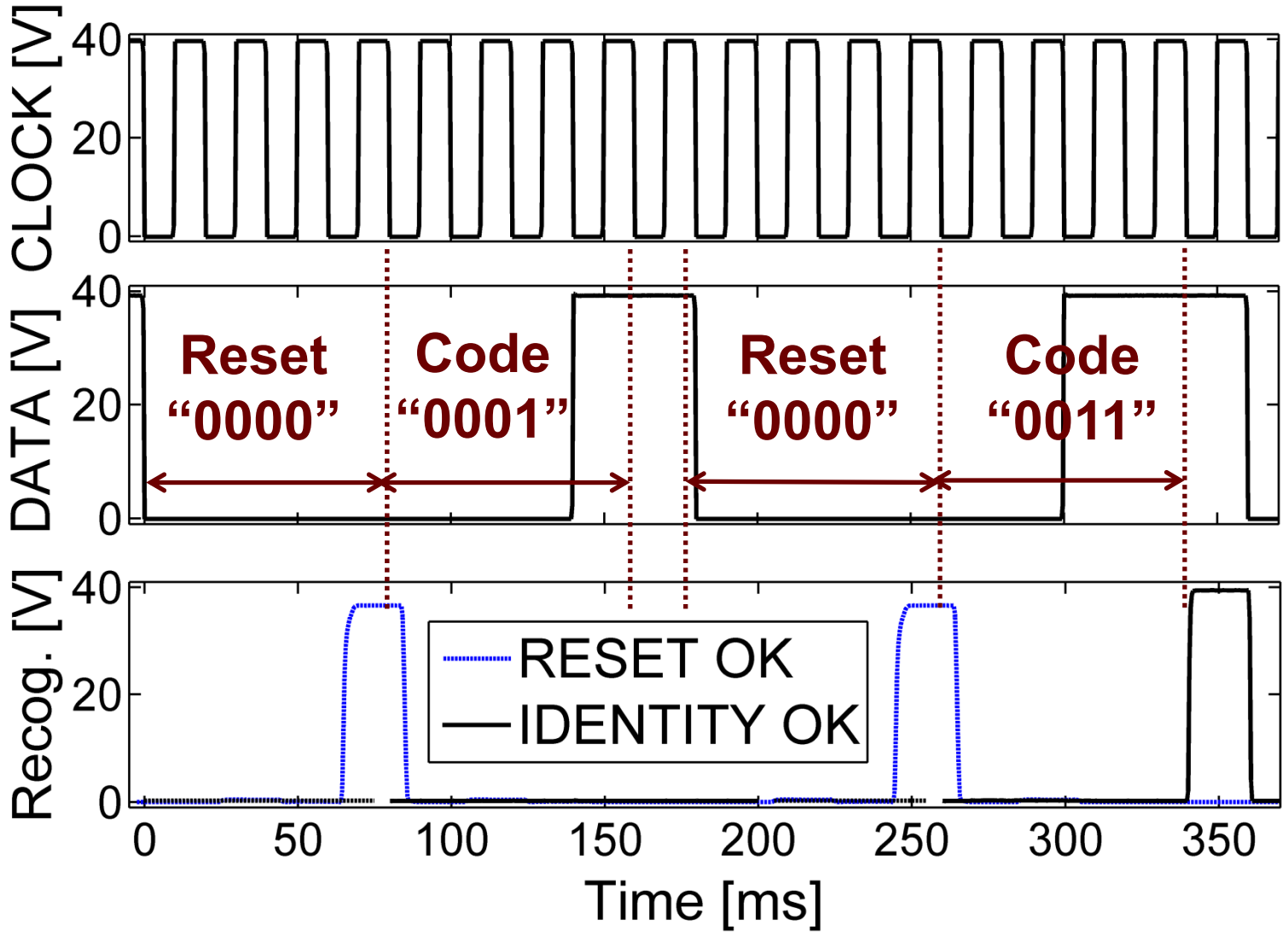
Code recognition unit: Identity Verification Module



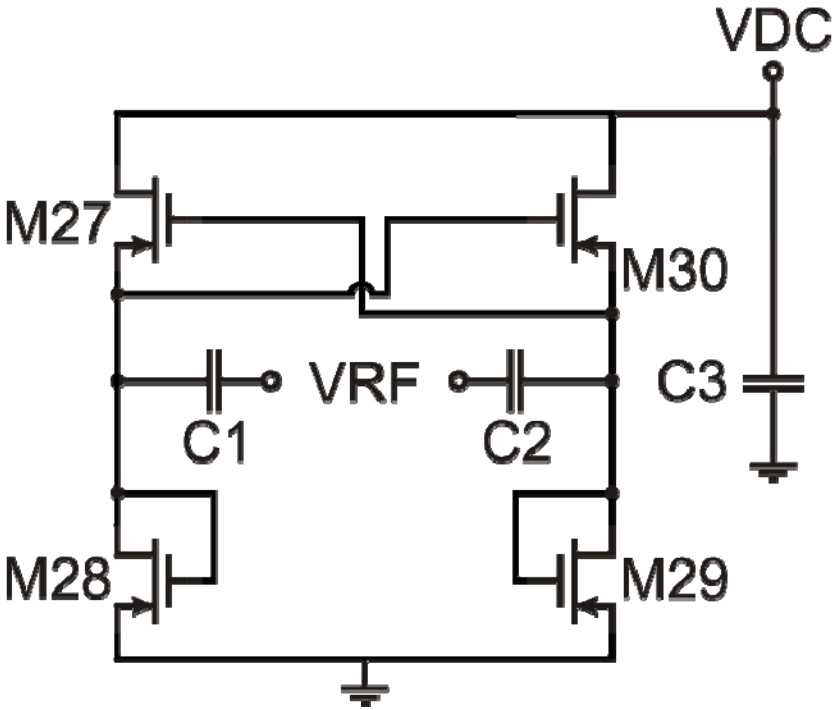
IVM performs identity comparison with the built-in logic array:

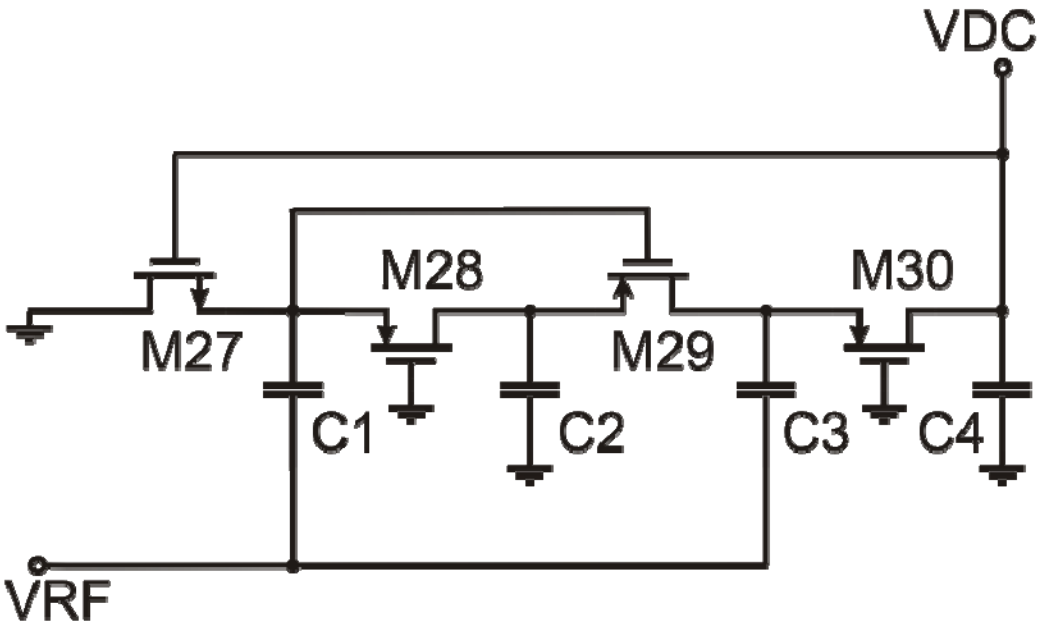
if DATA = "CODE" then ID_OK = "1"

Code recognition unit: measurements



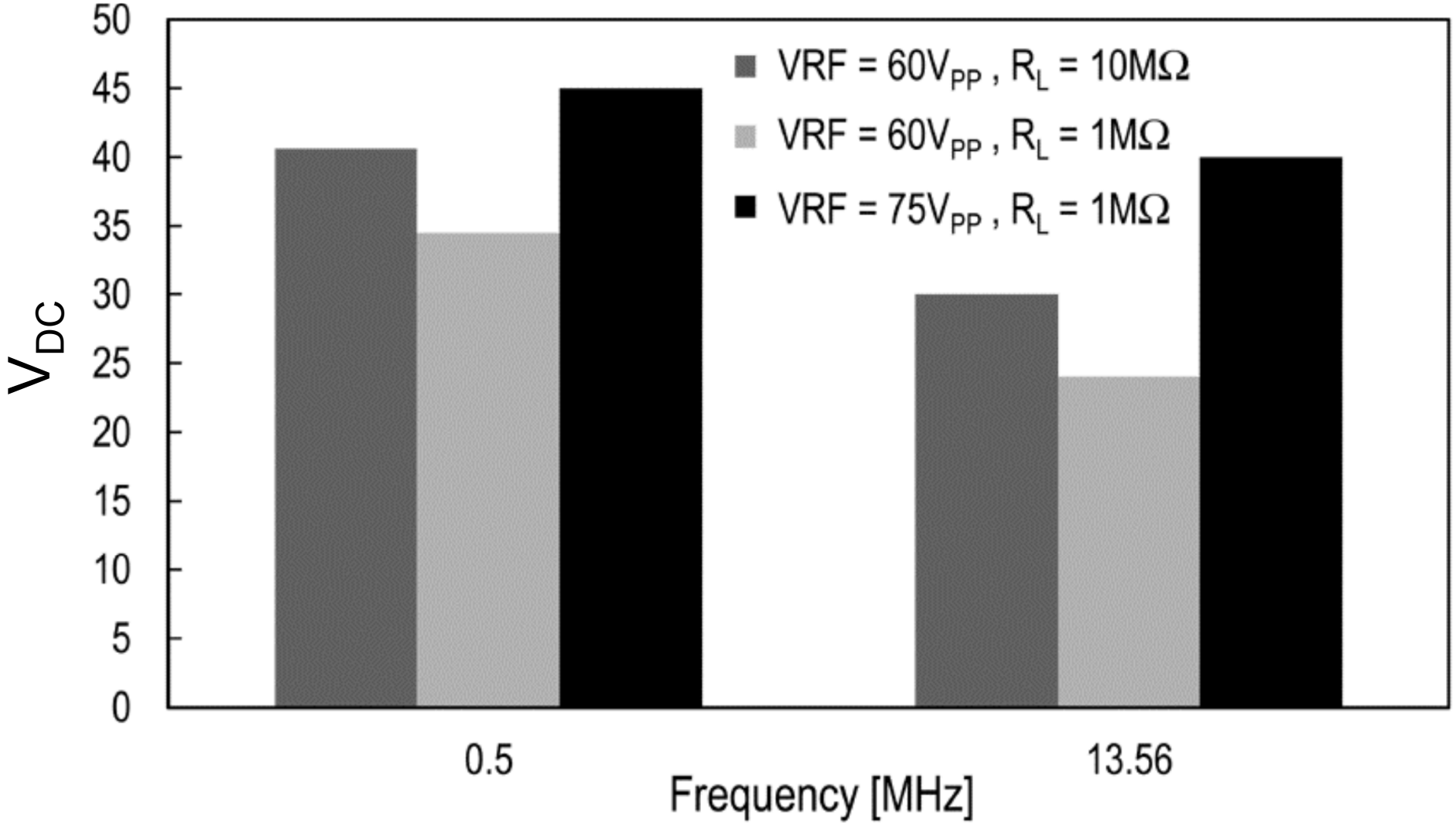
Rectifier: Full-wave versus 4-stage





RF [MHz]	VRF [V_{PP}]	Load [MΩ]	Measured V_{DC} [V]	
			Full-wave	4-stage
0.5	60	10	21	40.6
13.56	60	10	16.5	30

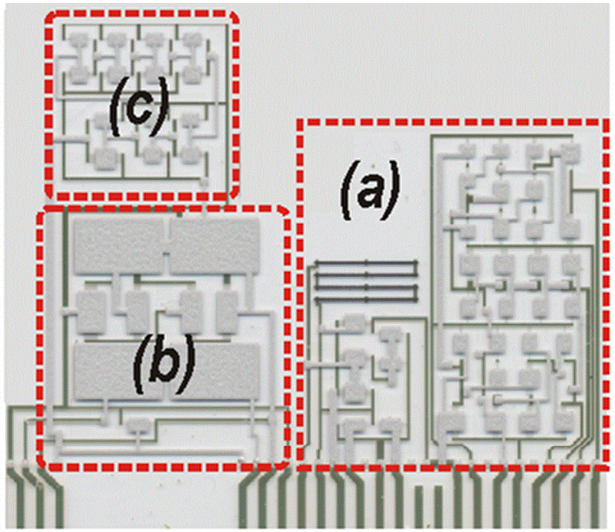
4-stage rectifier measurement

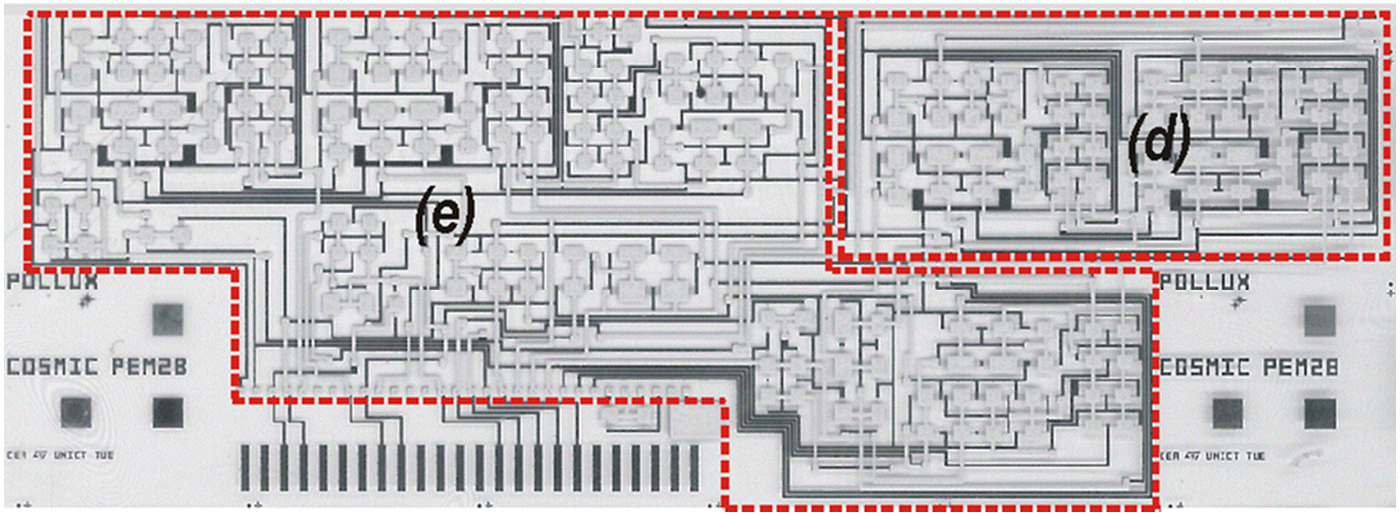


$I_{TOT} \approx 40\mu A @ V_{DD} = 40V \quad => \quad R_L \approx 1M\Omega$

Photos of measured RFID blocks

(a) RX front-end (370 mm²)
(b) Rectifier (280 mm²)
(c) Load modulator (145 mm²)
(d) Reset Module (490 mm²)
(e) Identity verification module (2000 mm²)





Conclusions

- ✓ New RFID tag architecture with a RX front-end
- ✓ All the blocks fully functional in a printed complementary-TFT technology
- ✓ First time ASK with 25% modulation index received using a printed C-OTFT technology

<u>..under development:</u>

- ➢ *Complete RFID circuitry and antenna has been fabricated and assembled*
- ➢ *Testing of the whole system will be soon performed!*

Acknowledgments

The authors would like to thank P. Battiato, S. Cantella, E. Cintolo, A. Castorina and G. Maiellaro.

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Thank you for your attention!

For any question please contact me at
vfiore@dieei.unict.it.

A GaN 3x3 Matrix Converter Chipset with Drive-by-Microwave Technologies

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Hiroyuki Handa, Yuji Kudoh, Hiroaki Ueno,
Masahiro Ishida, Nobuyuki Otsuka, and Daisuke Ueda

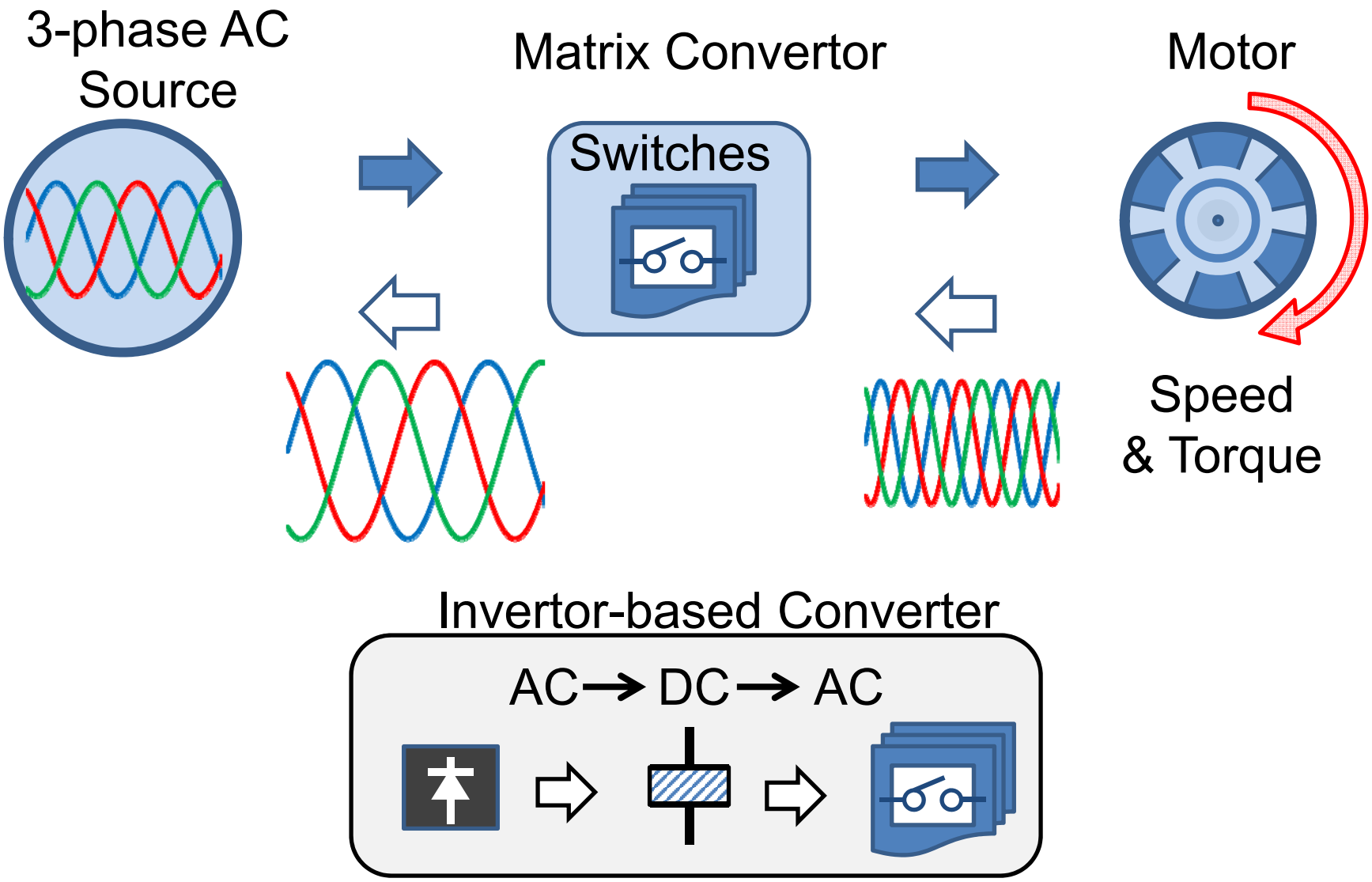
Panasonic Corporation

Panasonic

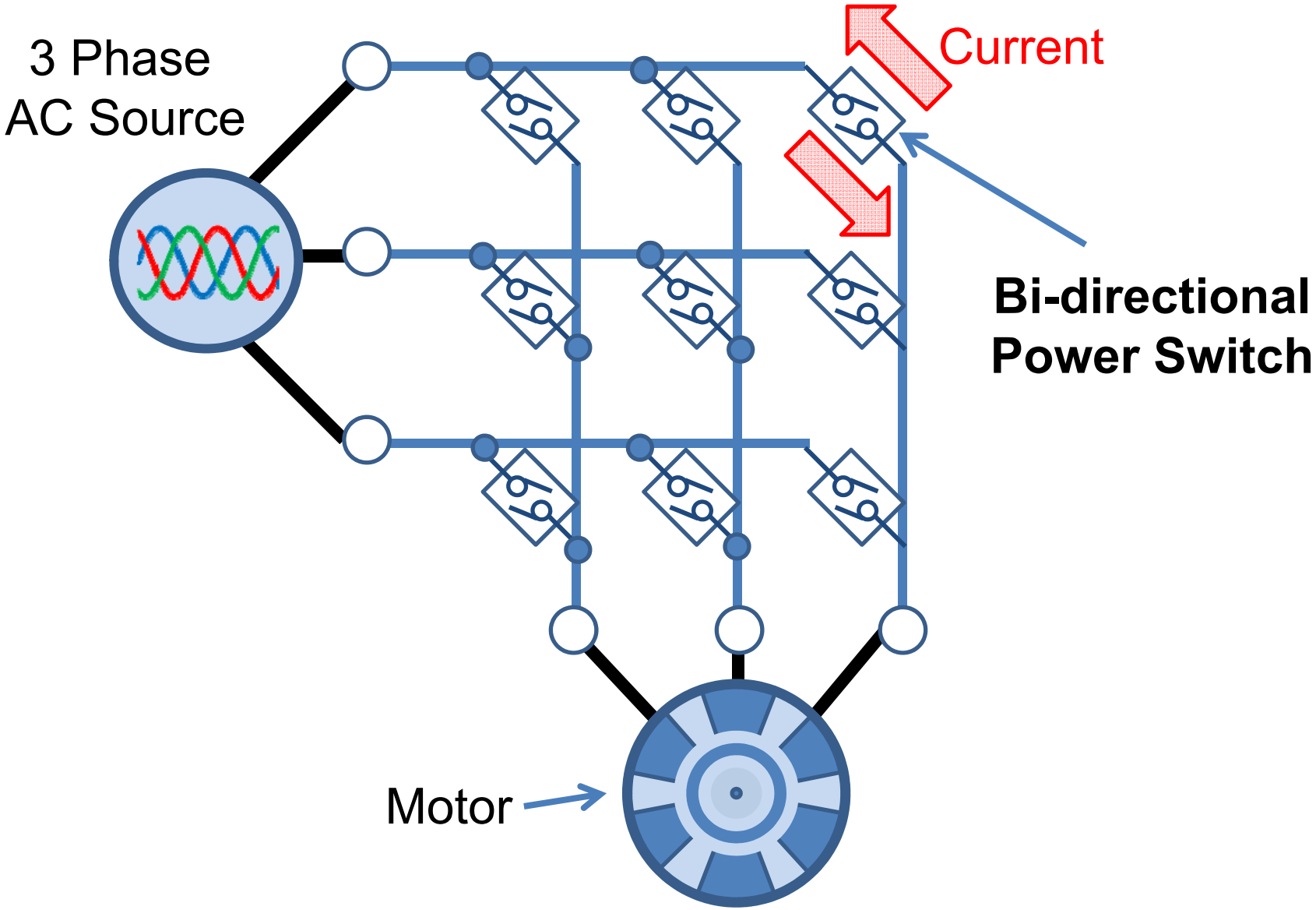
OUTLINE

- Introduction : Matrix Convertor for Motor Drive
- Approaches : Drive-by-Microwave (DBM) Technology
  - GaN Integrated Bi-directional Power Switching Chip
  - New Isolated Dividing Coupler
  - Gate Drive RF Transmitter Chip
- System : Compact 3x3 Matrix Convector

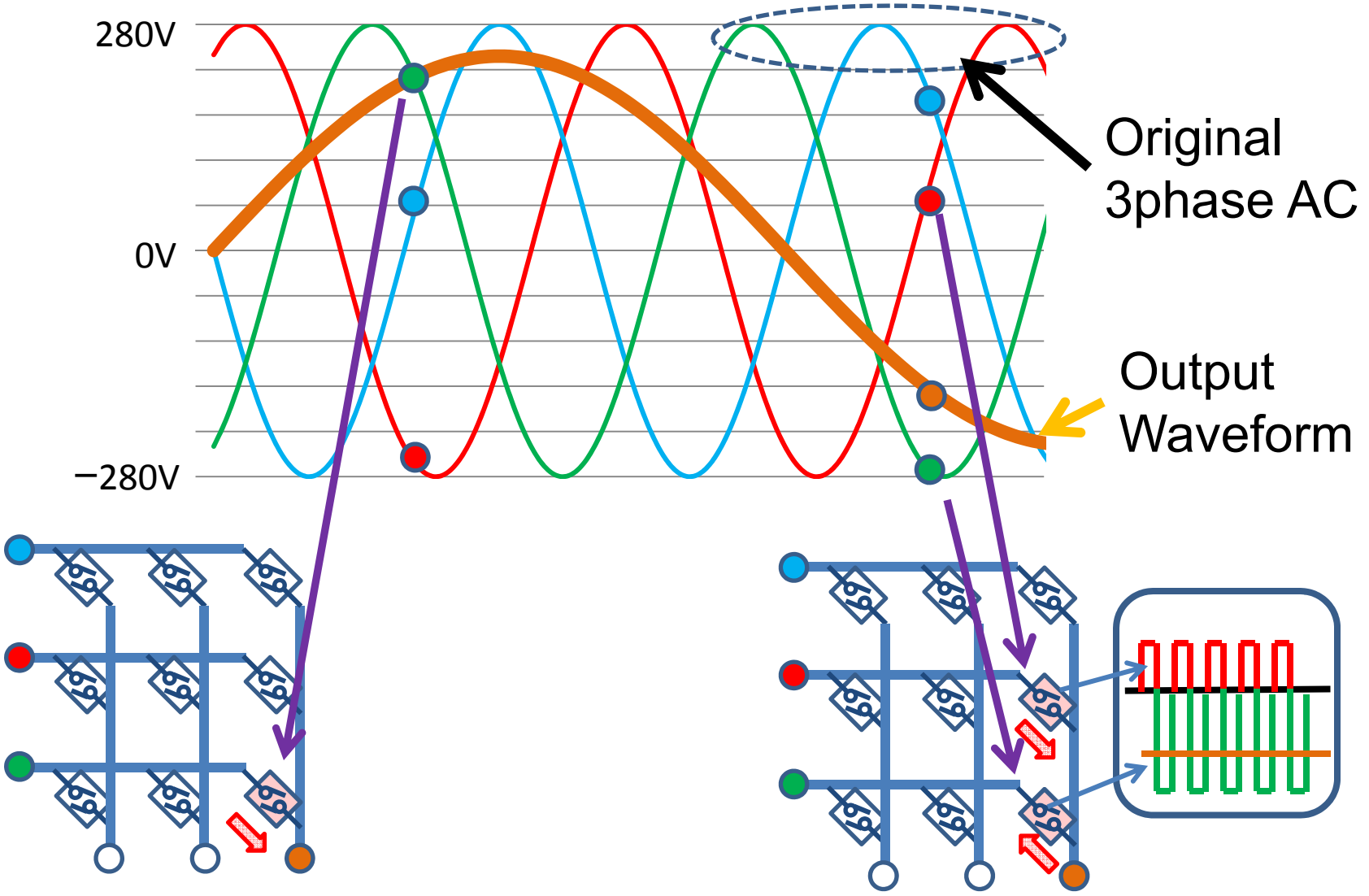
Power Convertor for Motor Drive



3x3 Matrix Convertor System



AC to AC Direct Conversion

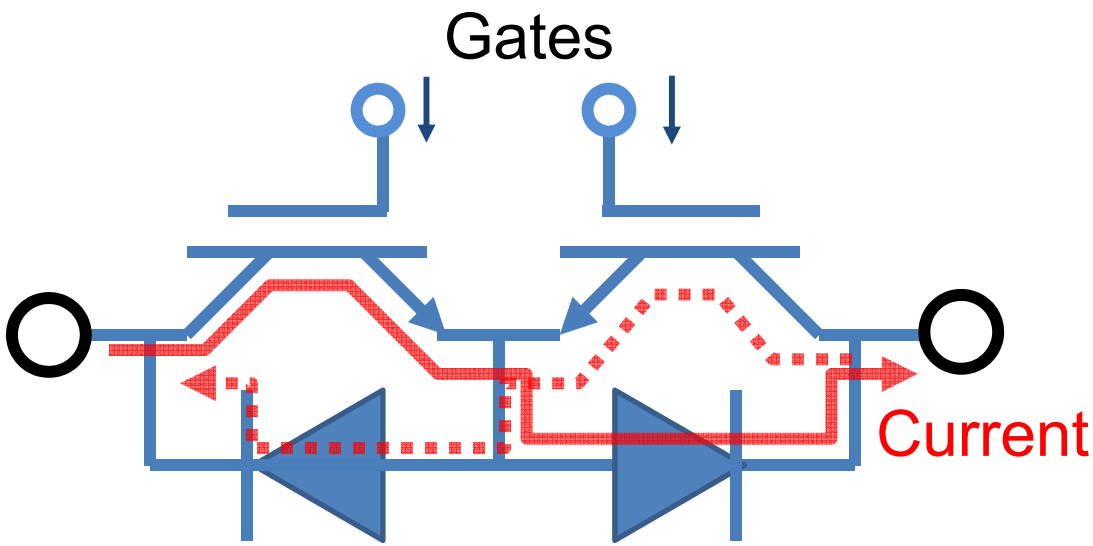


Issues on Conventional Matrix Convertor

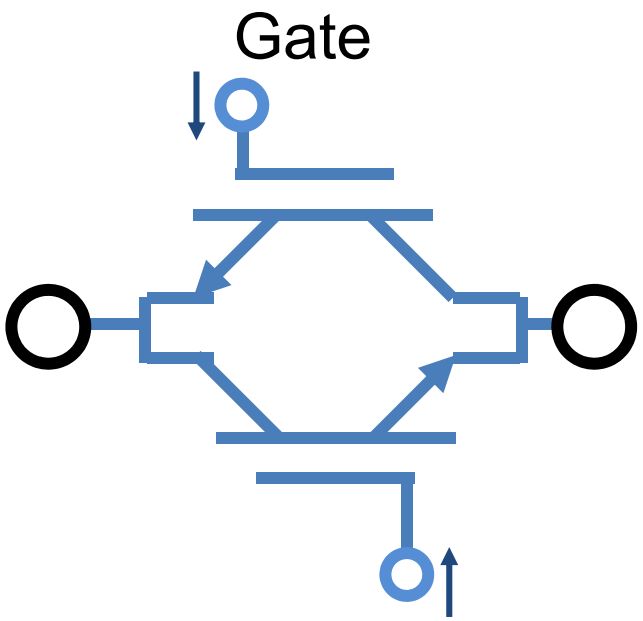
System size & Driver power consumption

- Bi-directional power switch with discrete components
  (2 Switches & 2 Diodes)
- Many gate control lines
  (18 channels for 9 bi-directional switches)
- Many isolated gate drivers with discrete components
  (18 Isolation supplies & Photo-couplers)

Conventional Bi-directional Switches



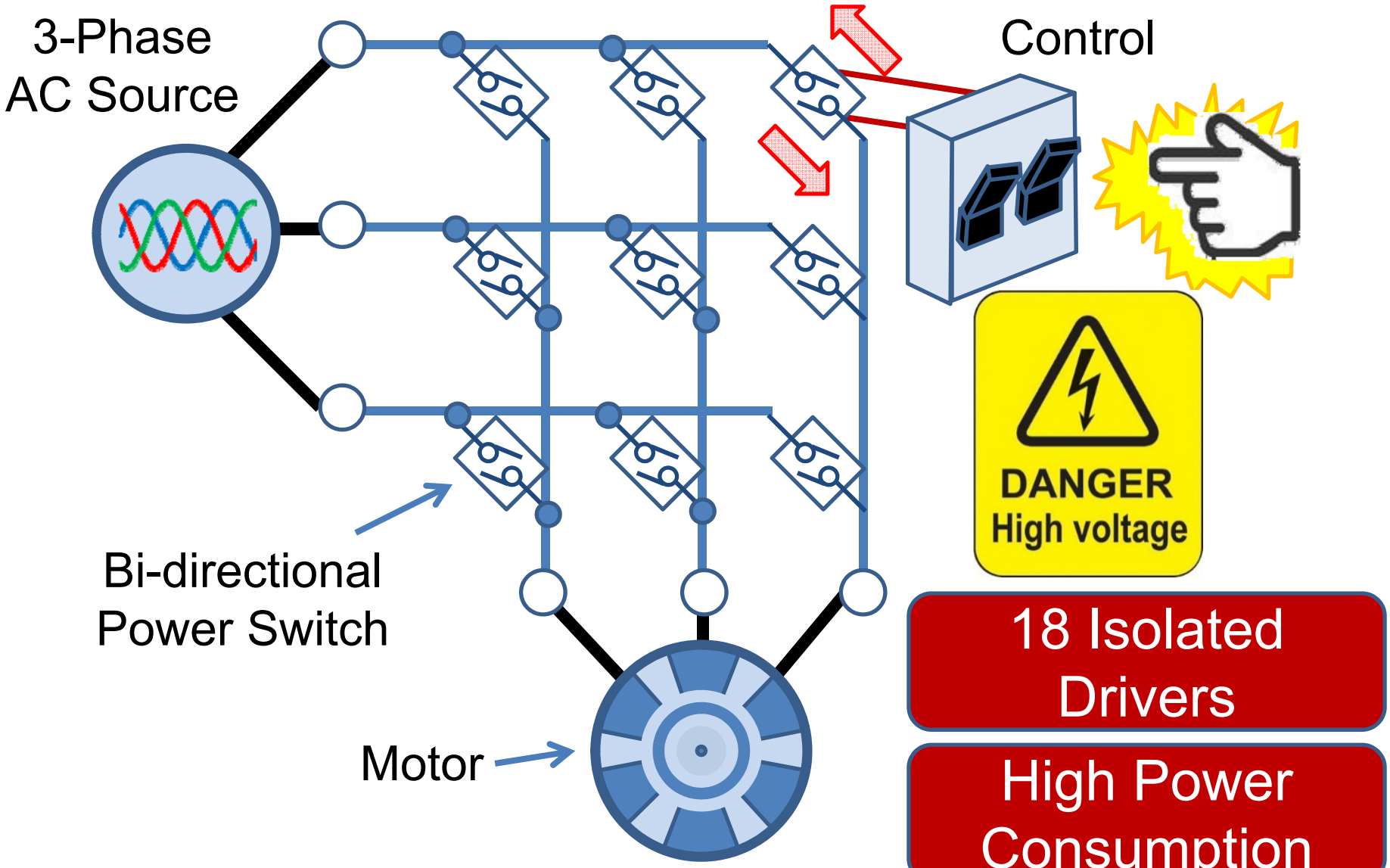
2 IGBTs & 2 Diodes



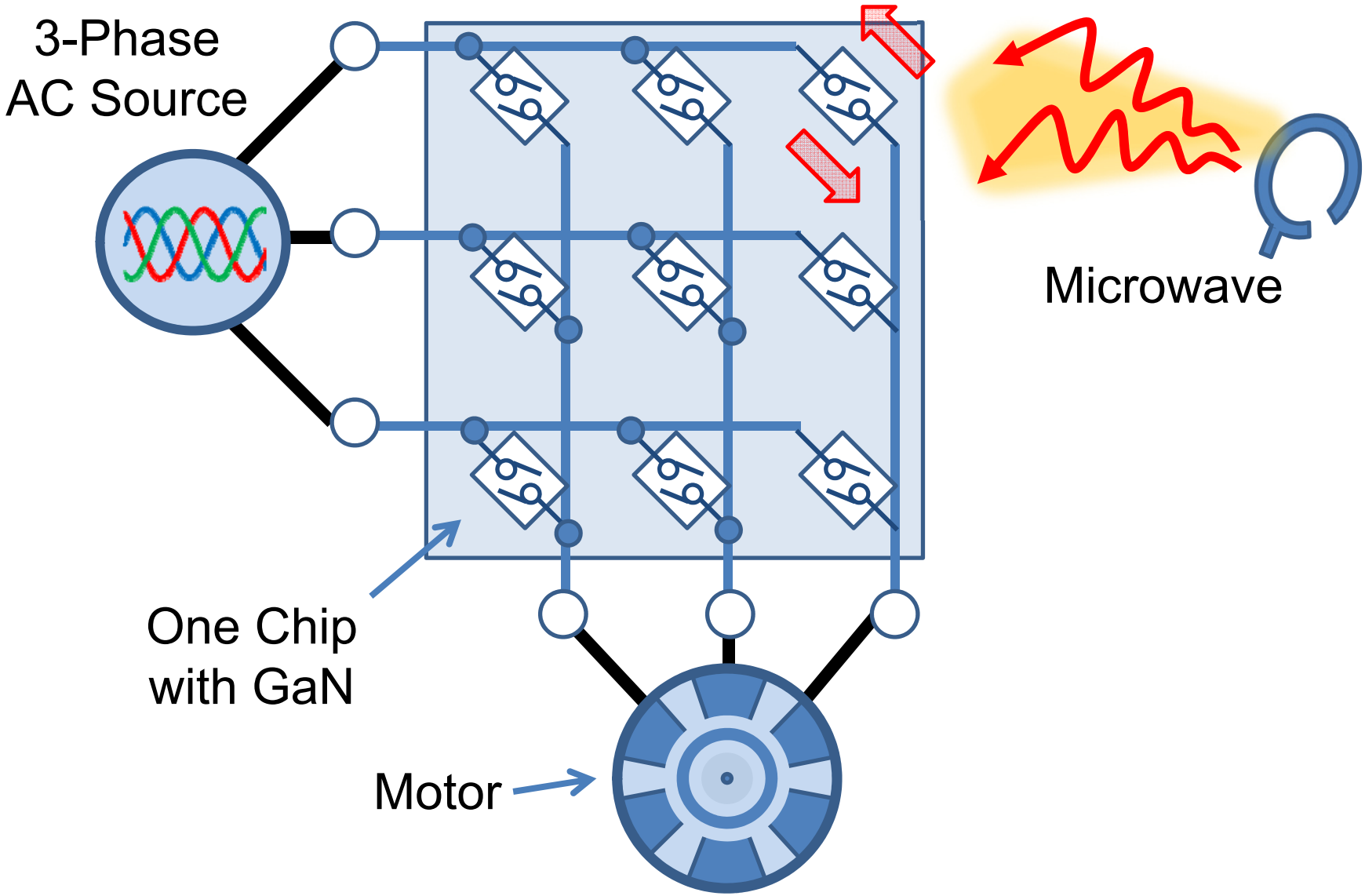
RB-IGBTs

Discrete Components

Requires Many Isolated Drivers



Microwave Isolated Control & One Chip

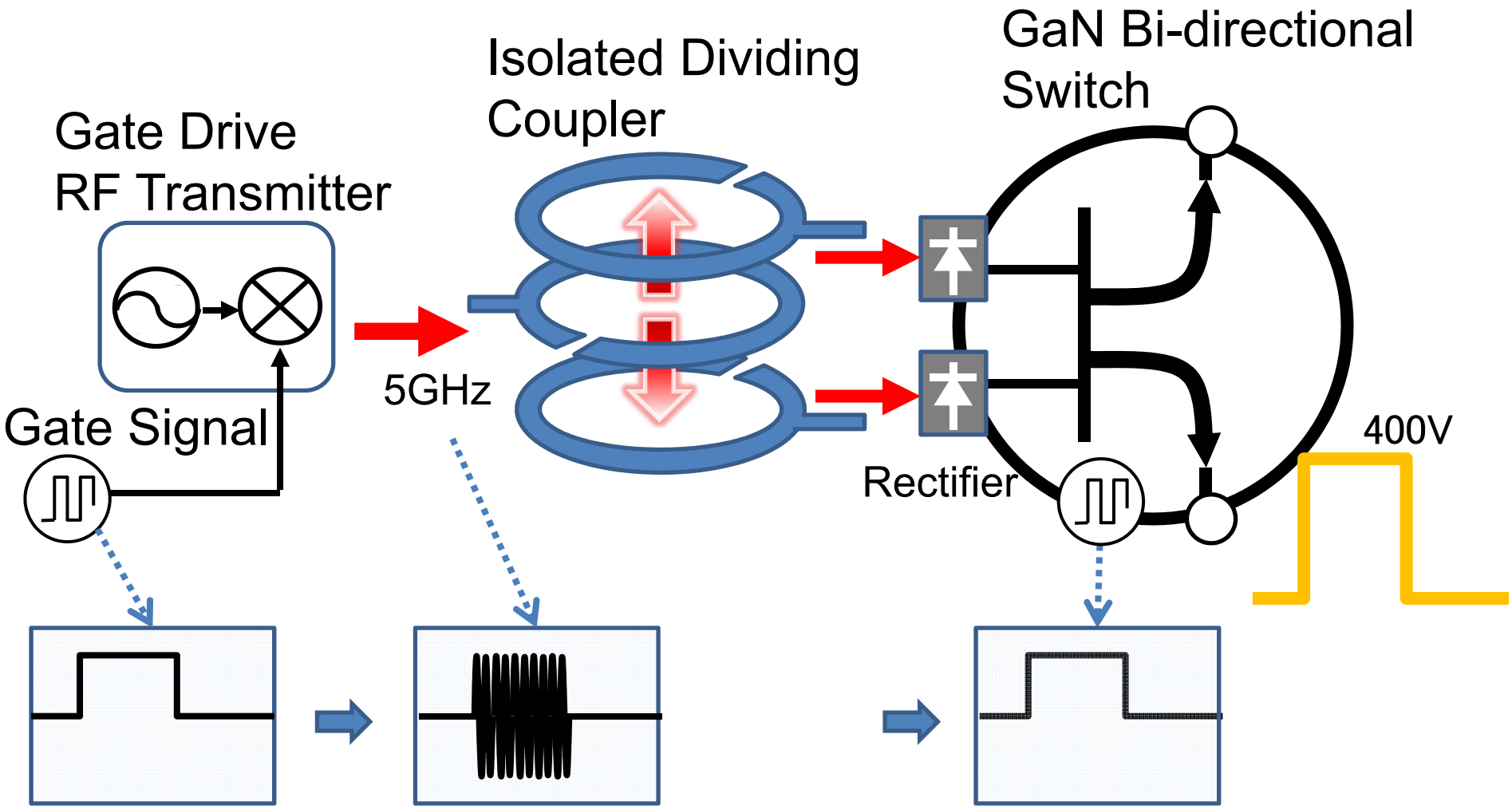


Approaches for Compact Matrix Convertor

- Problems ⇨ Solutions
  - Bi-directional power switch with discrete components
    - ⇨ GaN bi-directional switch & its integration
  - Many gate control lines
    - ⇨ Isolated dividing coupler (to reduce gate lines)
  - Many Isolated gate drivers with discrete components
    - ⇨ One-chip low consumption driver (for 9 SW's)

GaN Drive-by-Microwave (DBM) Technology

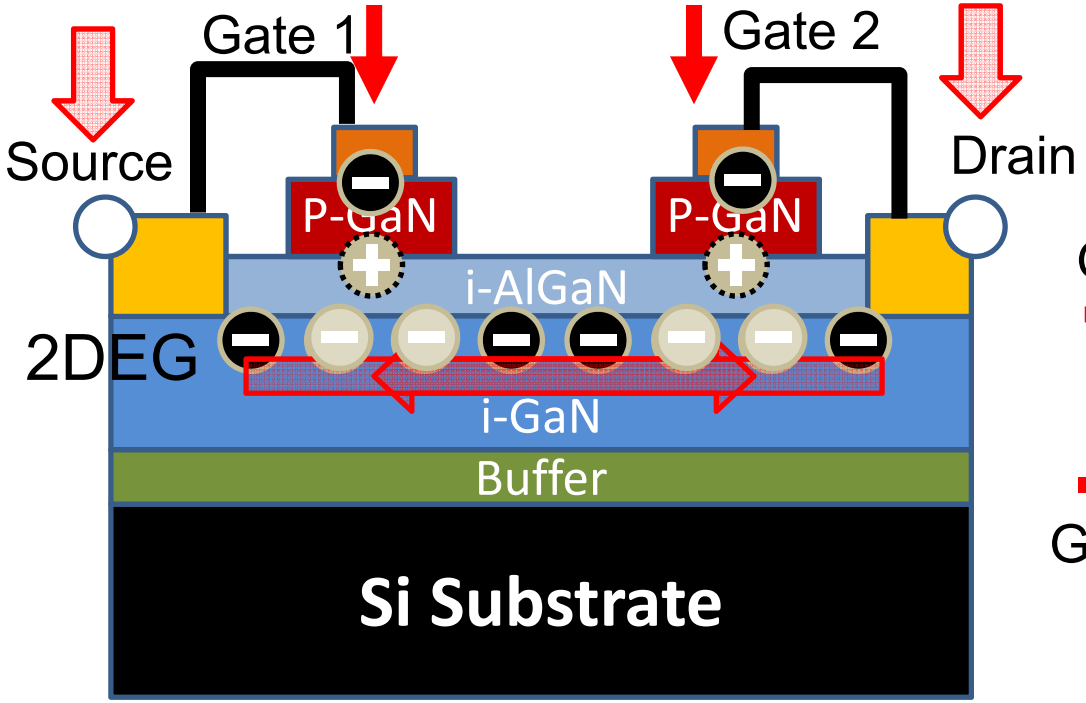
Microwave wireless power and signal transmission



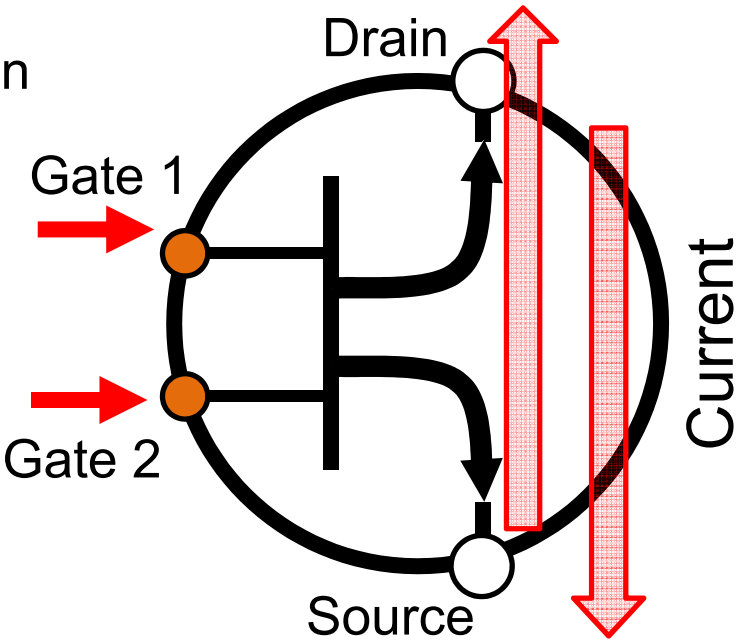
GaN Bi-directional Power Switch

Conventional : 2 Switches & 2 Diodes

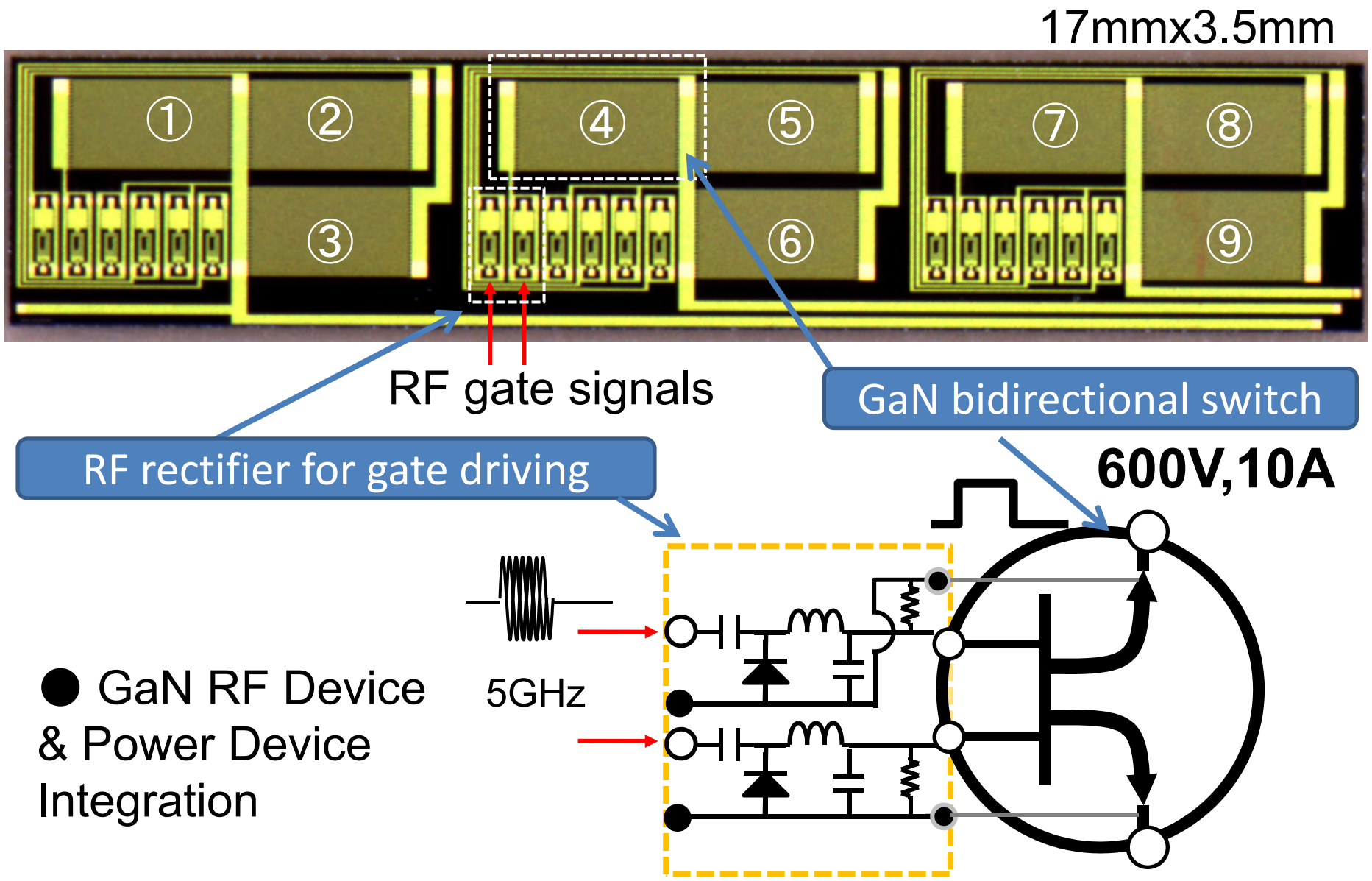
Gate Injection Transistor (GIT)



One Device

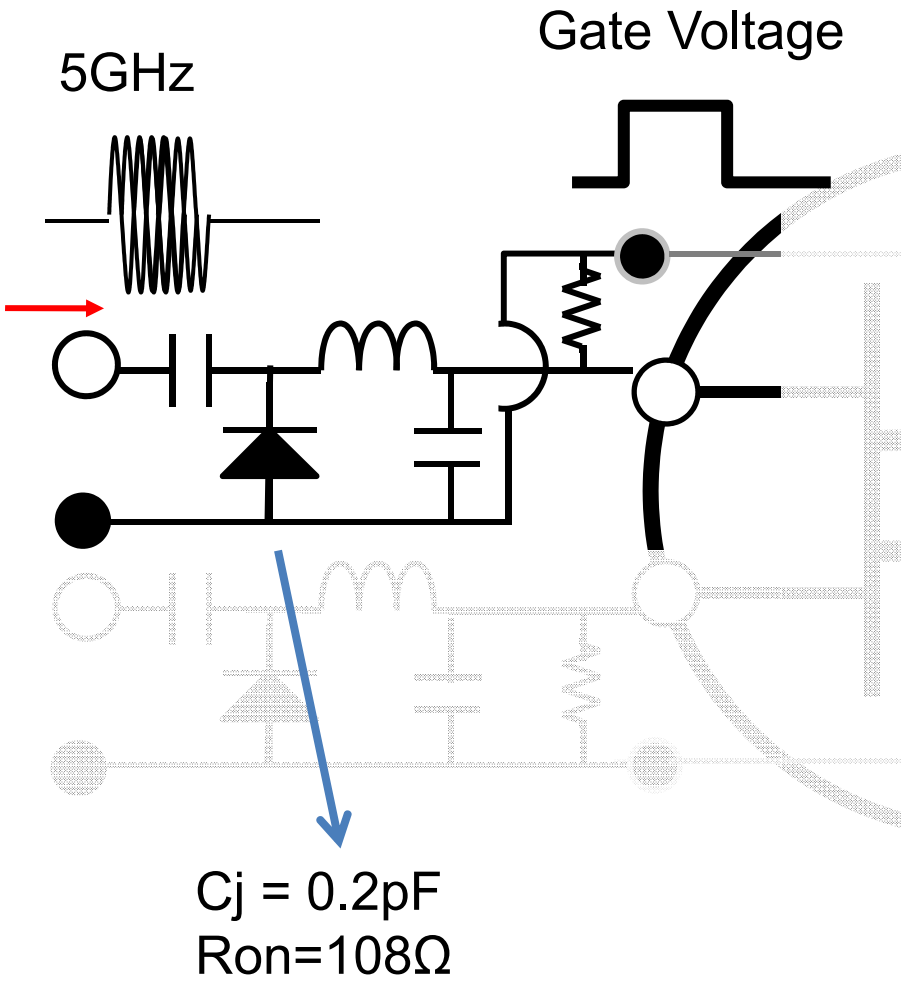


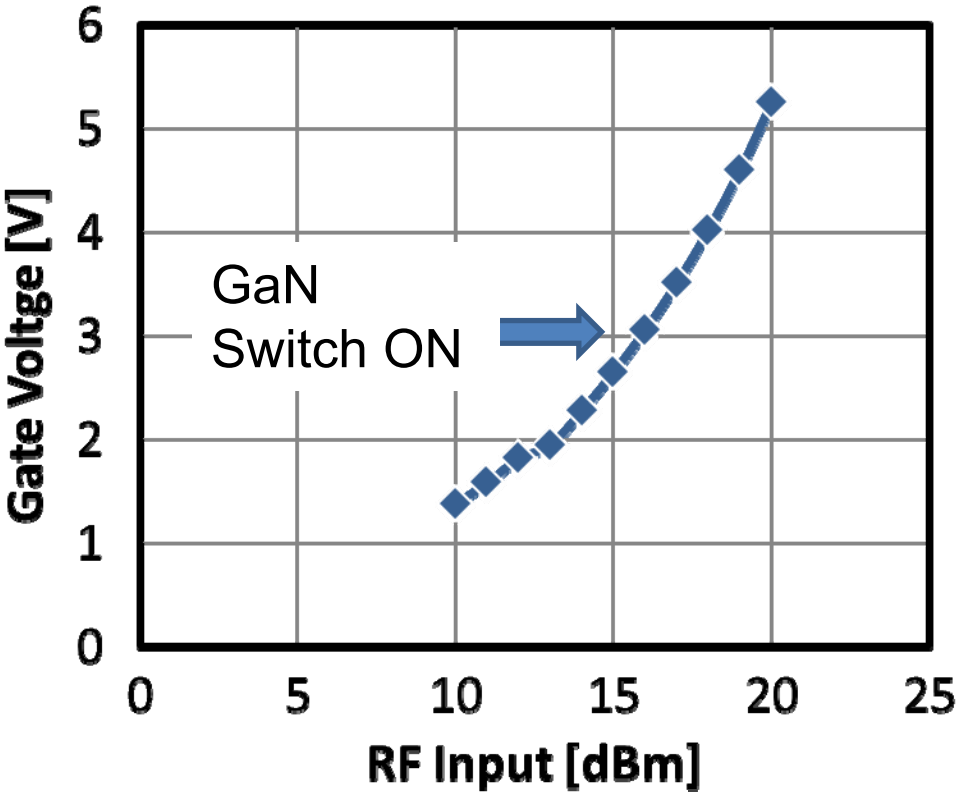
3x3 Integrated Bi-directional Switch



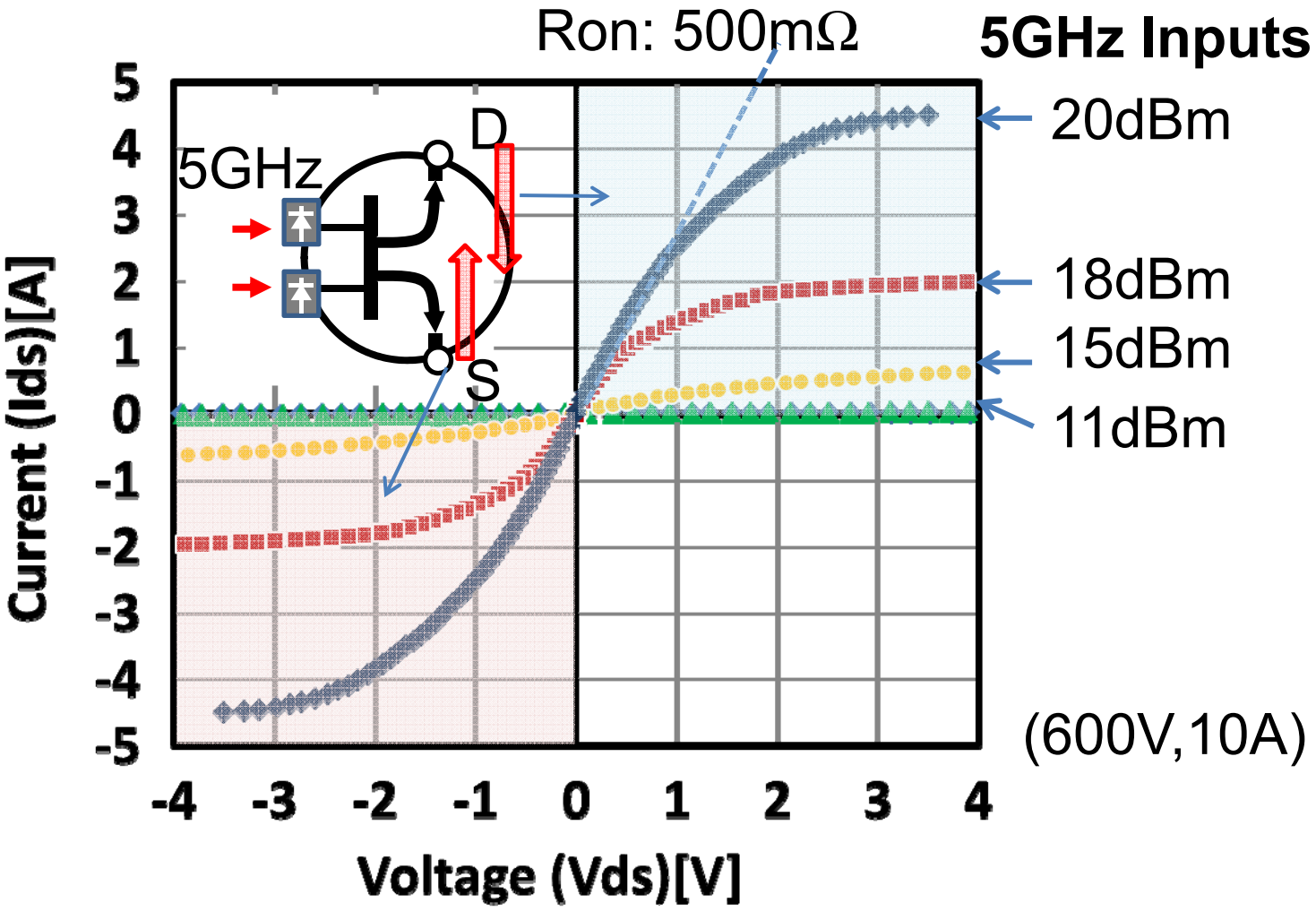
● GaN RF Device & Power Device Integration

RF Rectifier in GaN Bi-directional Switch



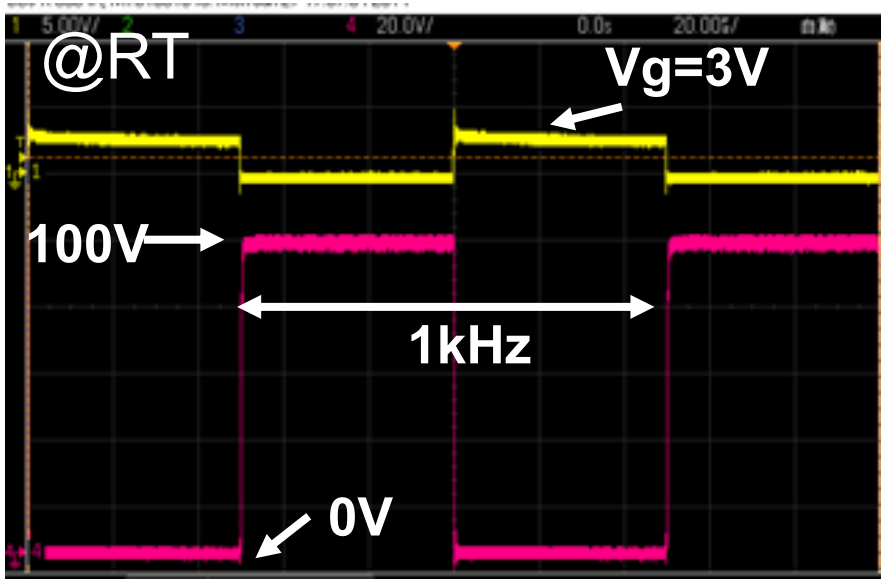


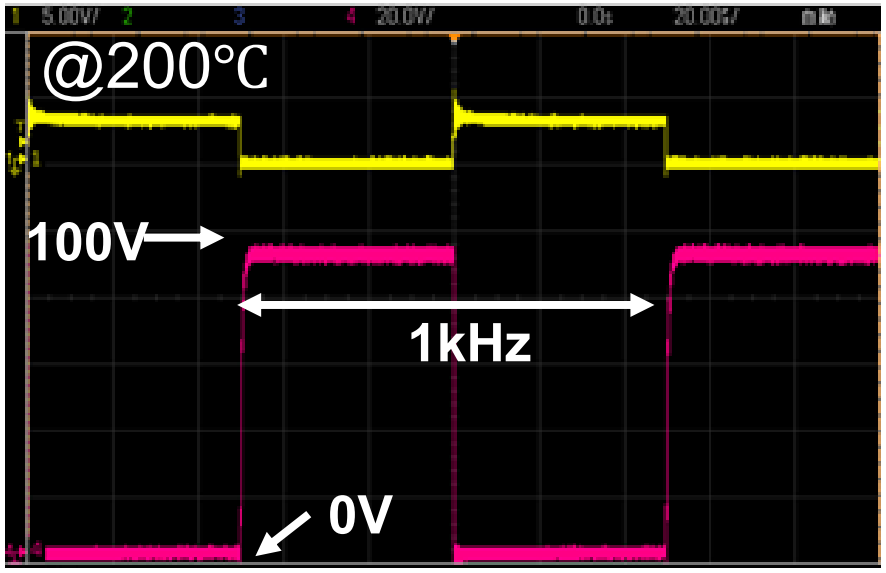
RF Triggered Bi-directional Switch

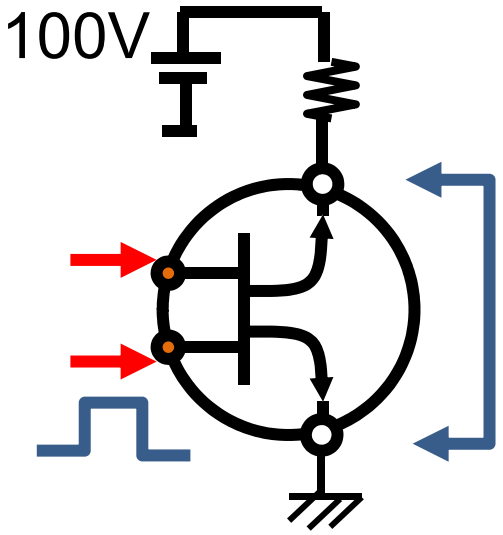


- Bi-directional operation by RF signal inputs

Switching Operation at High Temperature



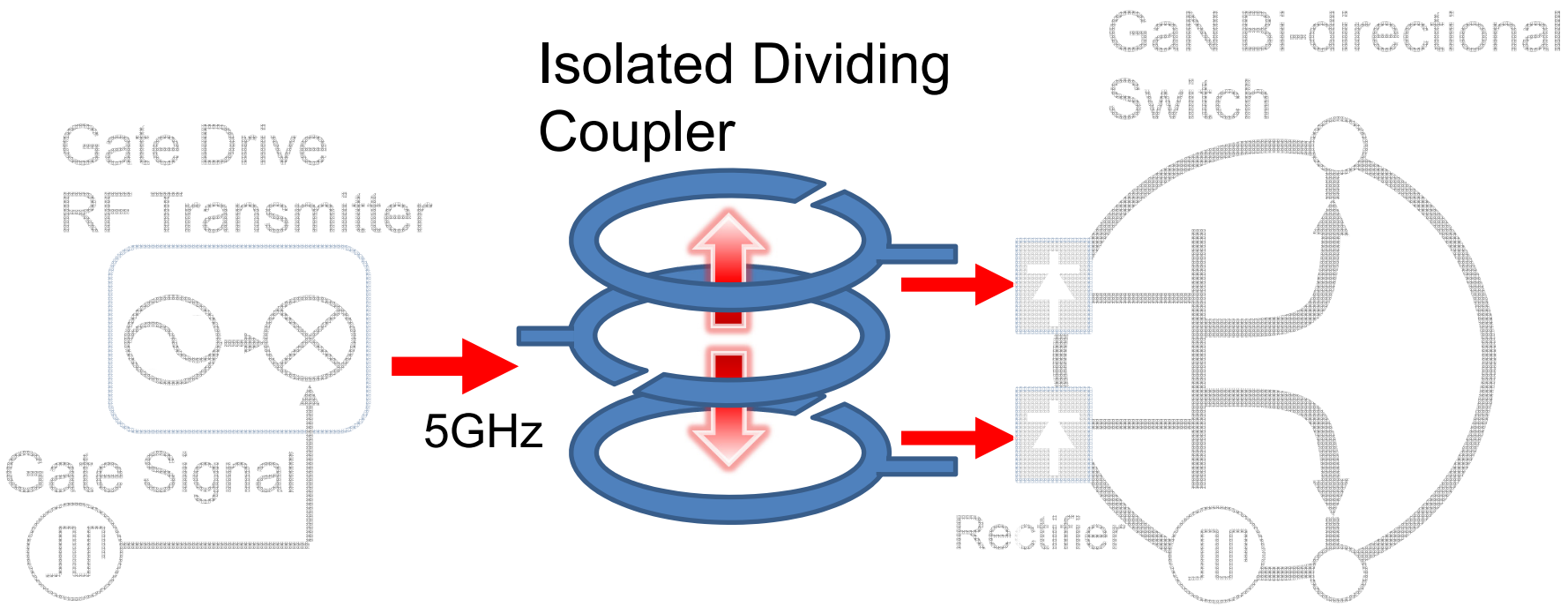




- Operation at high temperature
- Heat suppression by low-loss

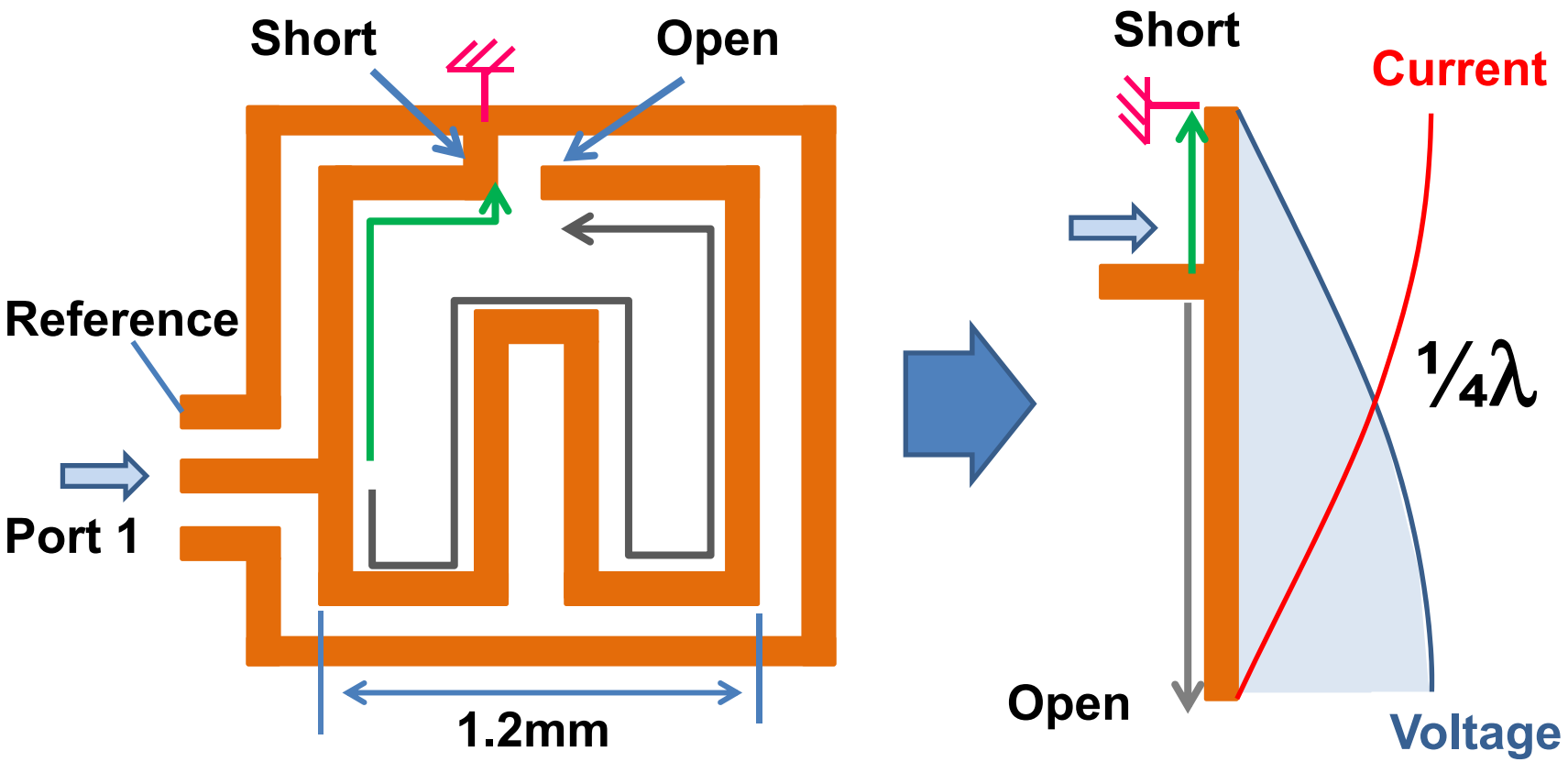
Small Heat Sink

1x2 Isolated Dividing Coupler



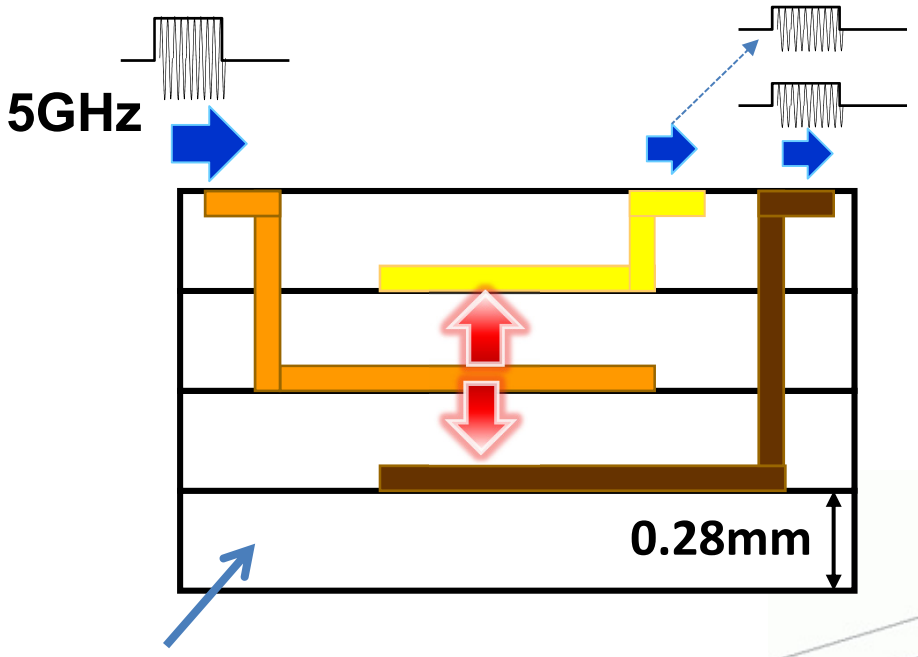
Gate Line Reduction by Half

Isolated Dividing Coupler for 5 GHz Signal



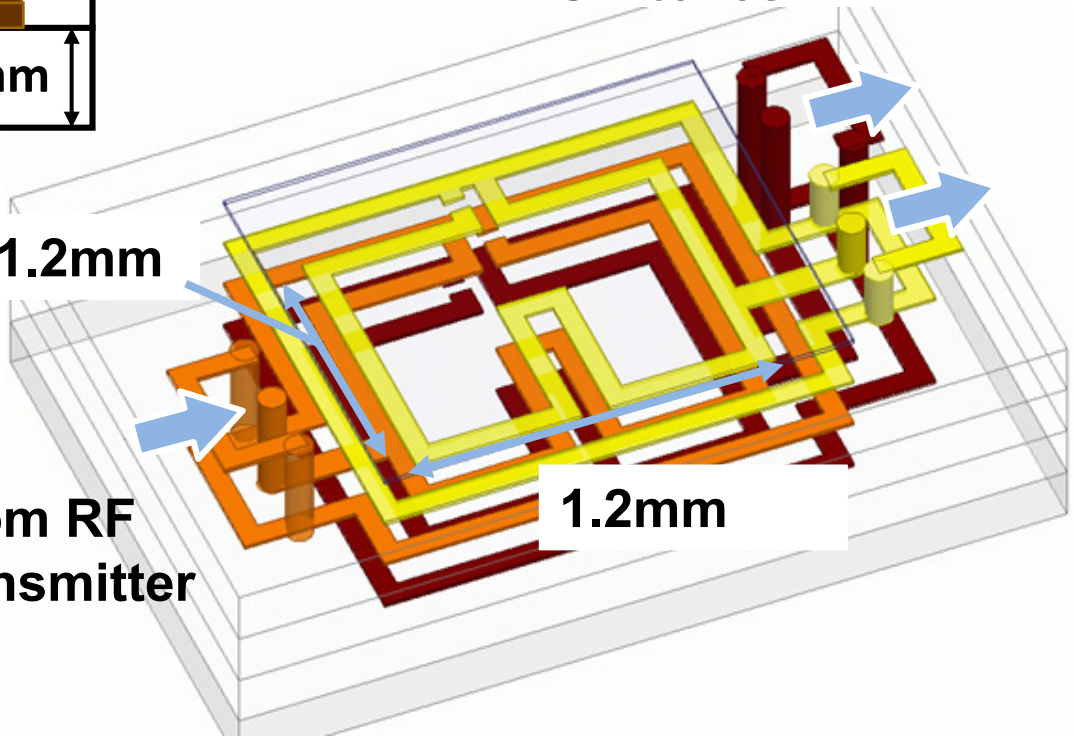
Short and Open edged ¼ λ resonator

Electro-Magnetic Resonant Coupling



- 3 Resonators Stacking

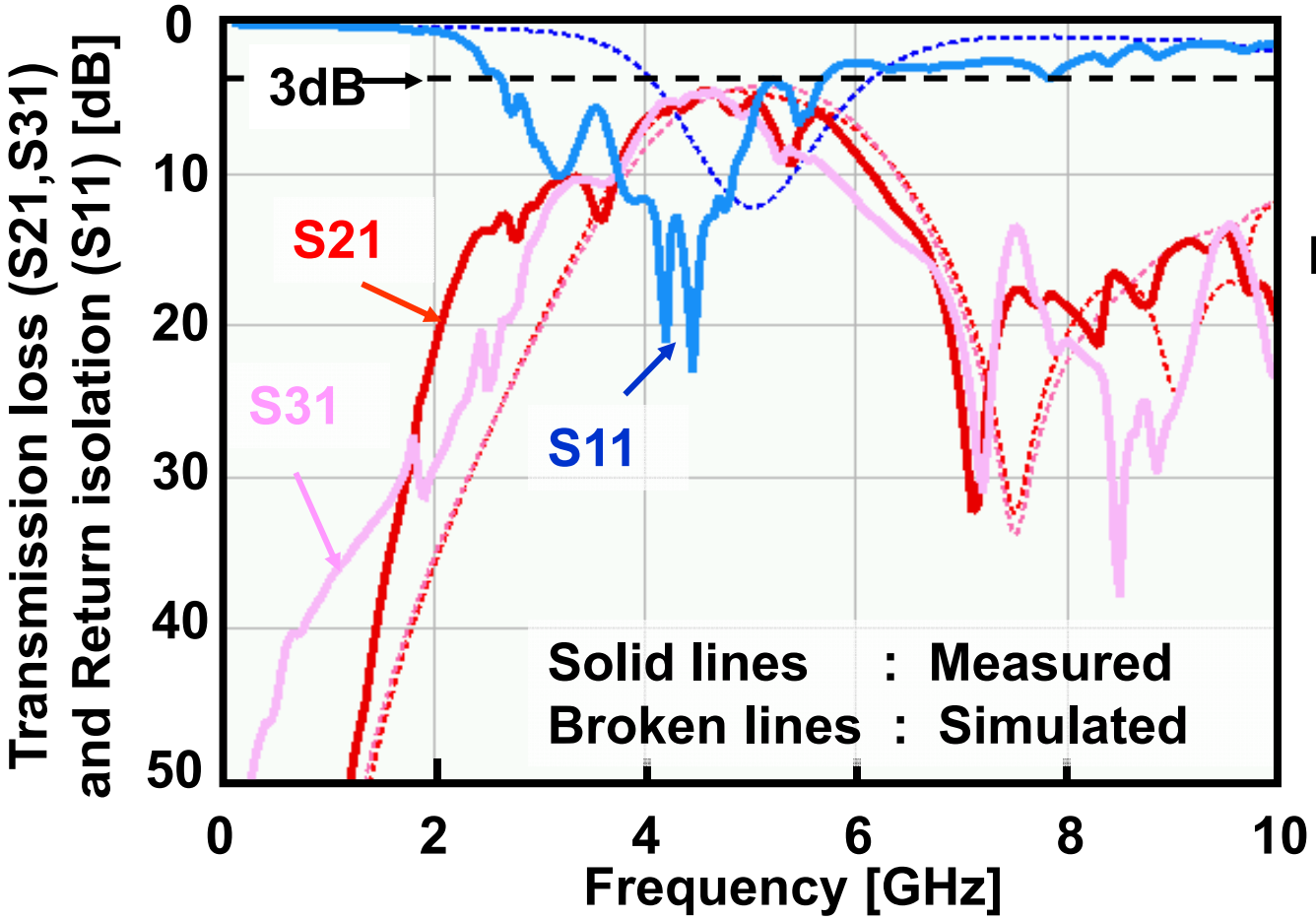
To Bi-directional Switches

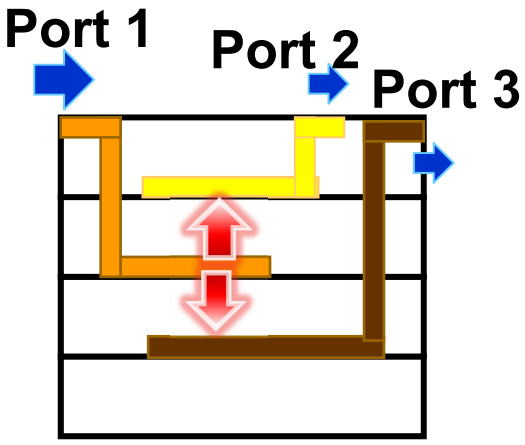


Low-cost Printed Circuits Board(P.C.B)

From RF transmitter

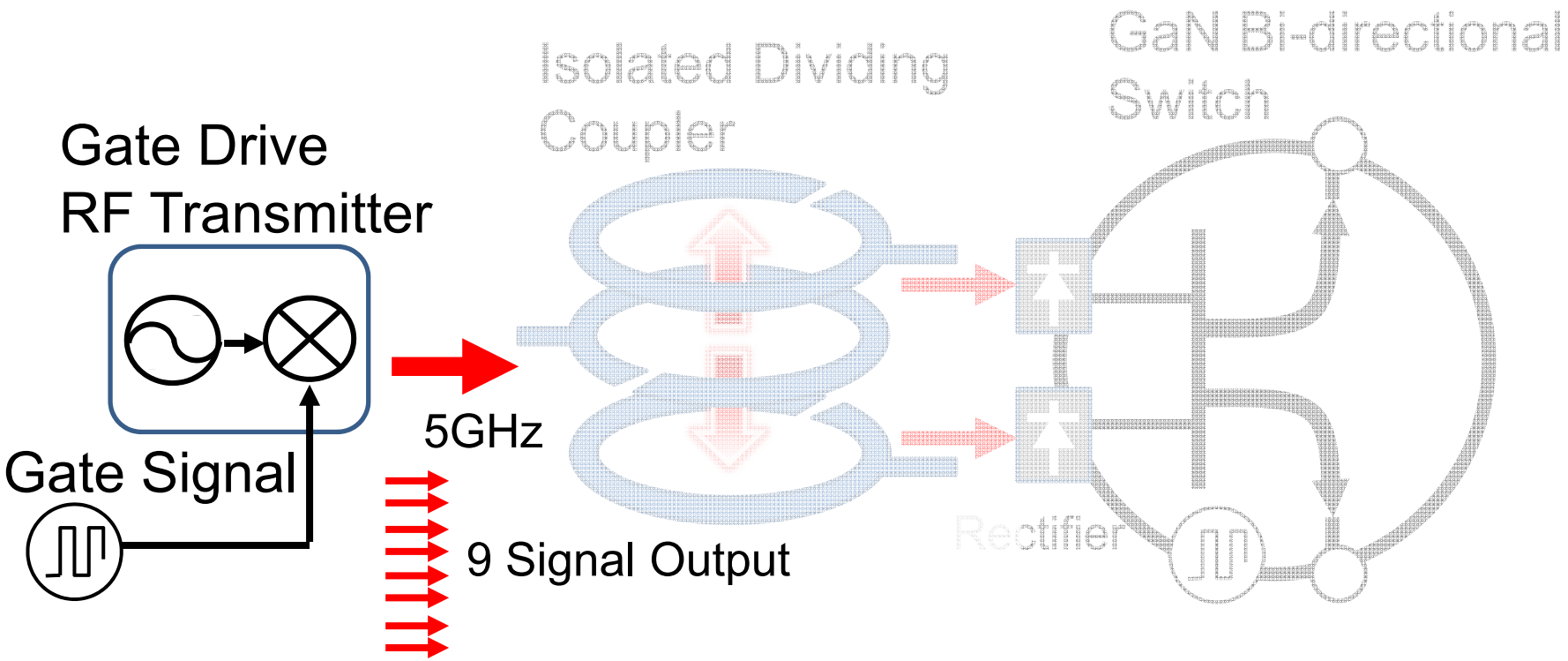
Coupler in Low-cost Printed Circuit Board





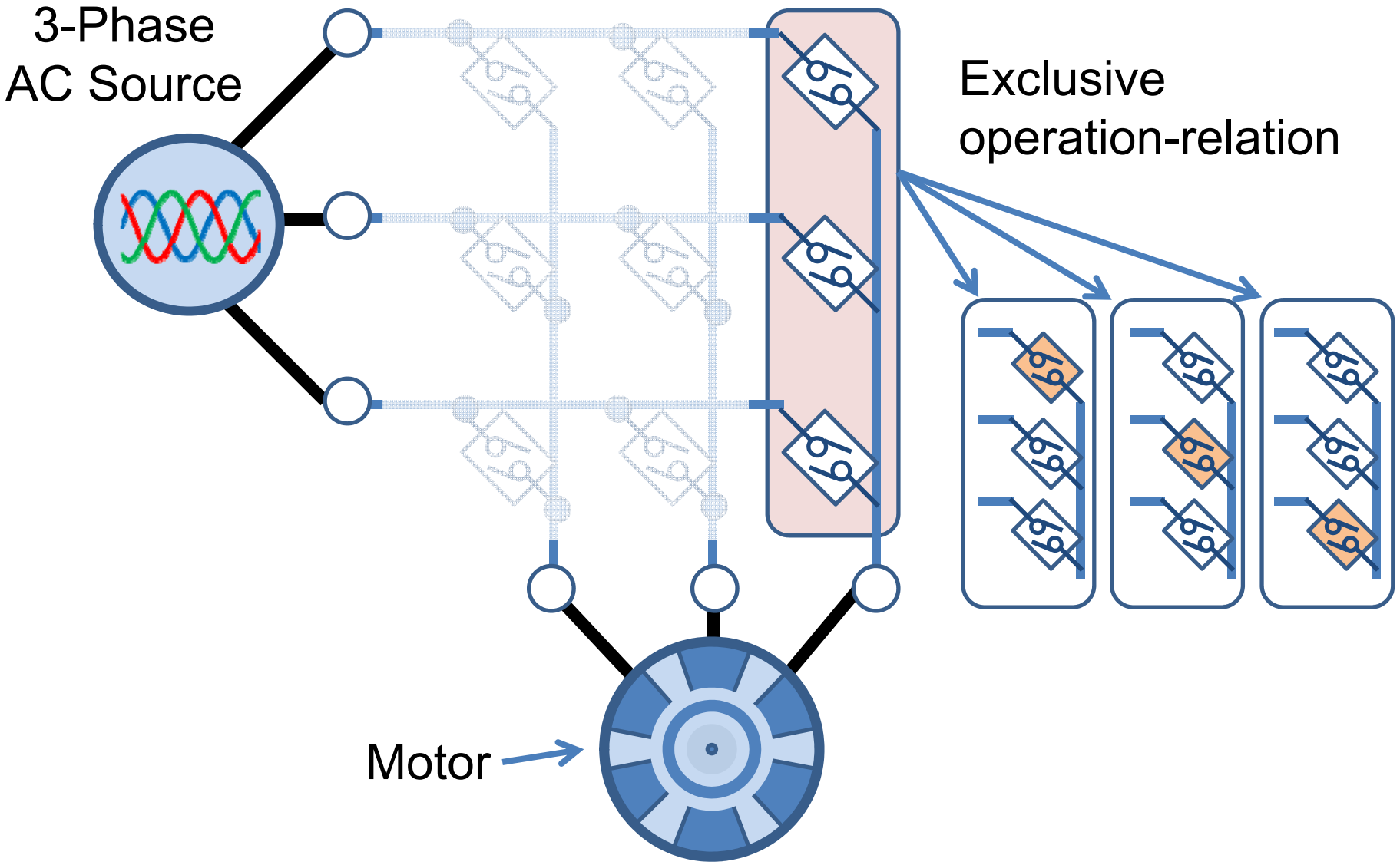
- Only 1.1 dB insertion loss
- Isolated voltage over 5.0kV

Gate Drive RF Transmitter



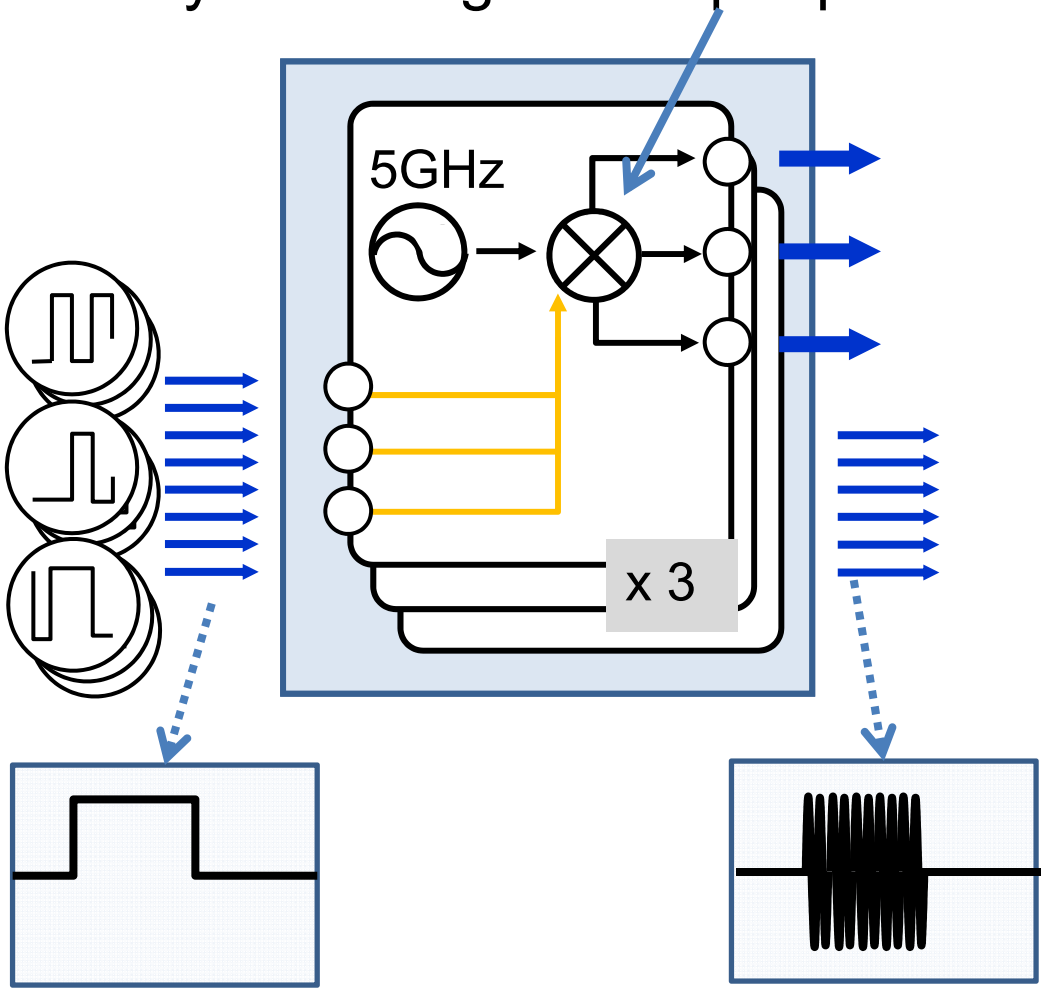
One-chip & Low Consumption Driver for 9 Switches

Exclusive Switching Operation

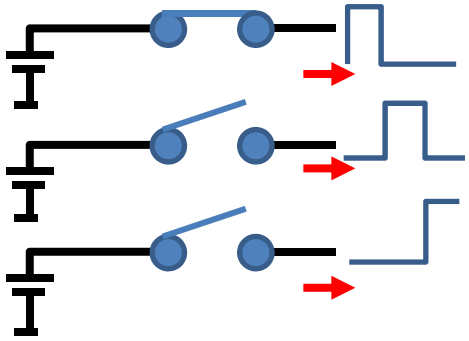


Low Consumption Gate Driver RF Transmitter

Signal Power Sharing
by switching the output ports

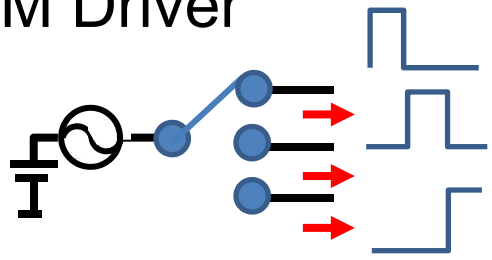


● Conventional



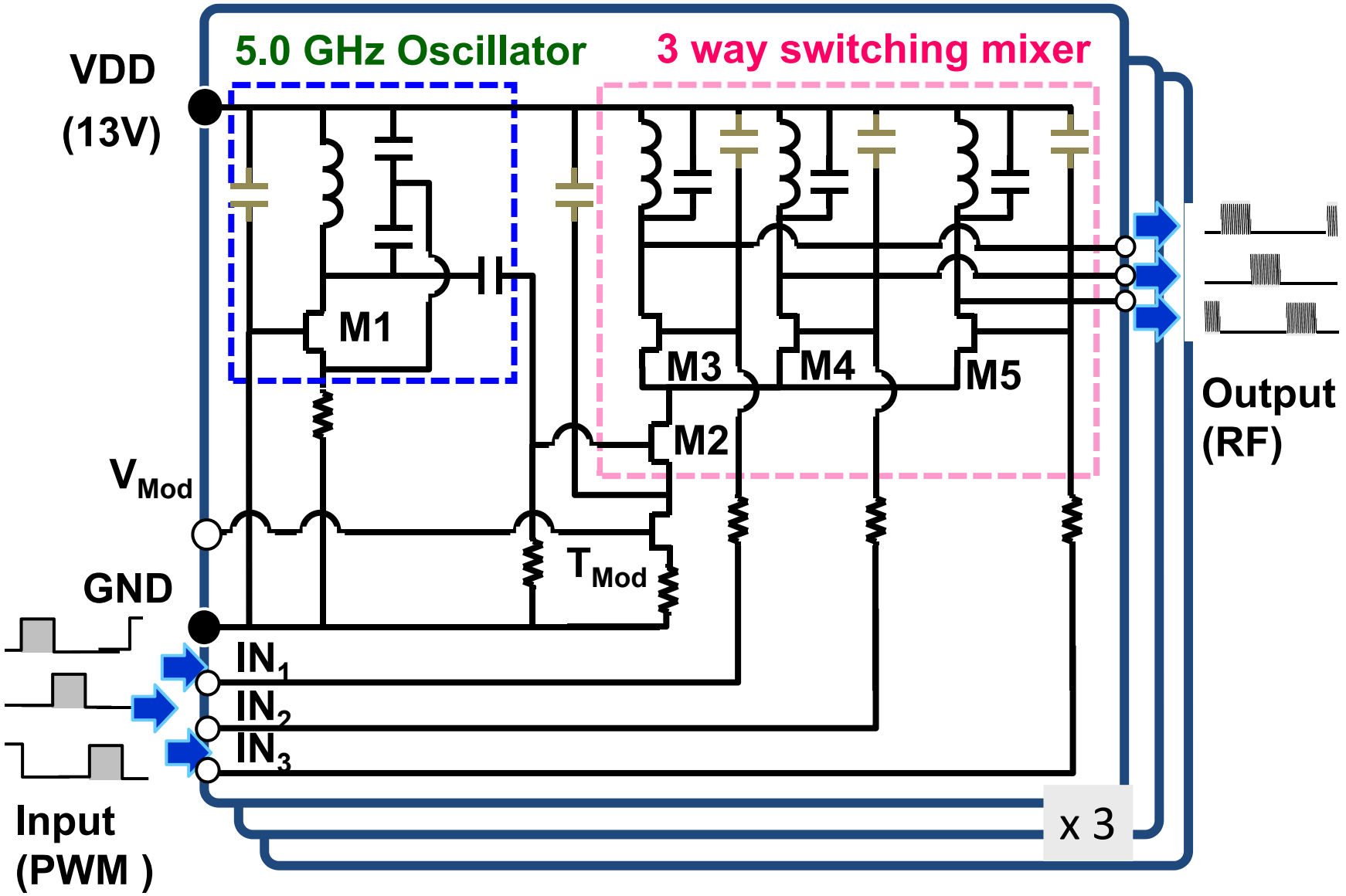
3 isolated
DC sources

● DBM Driver

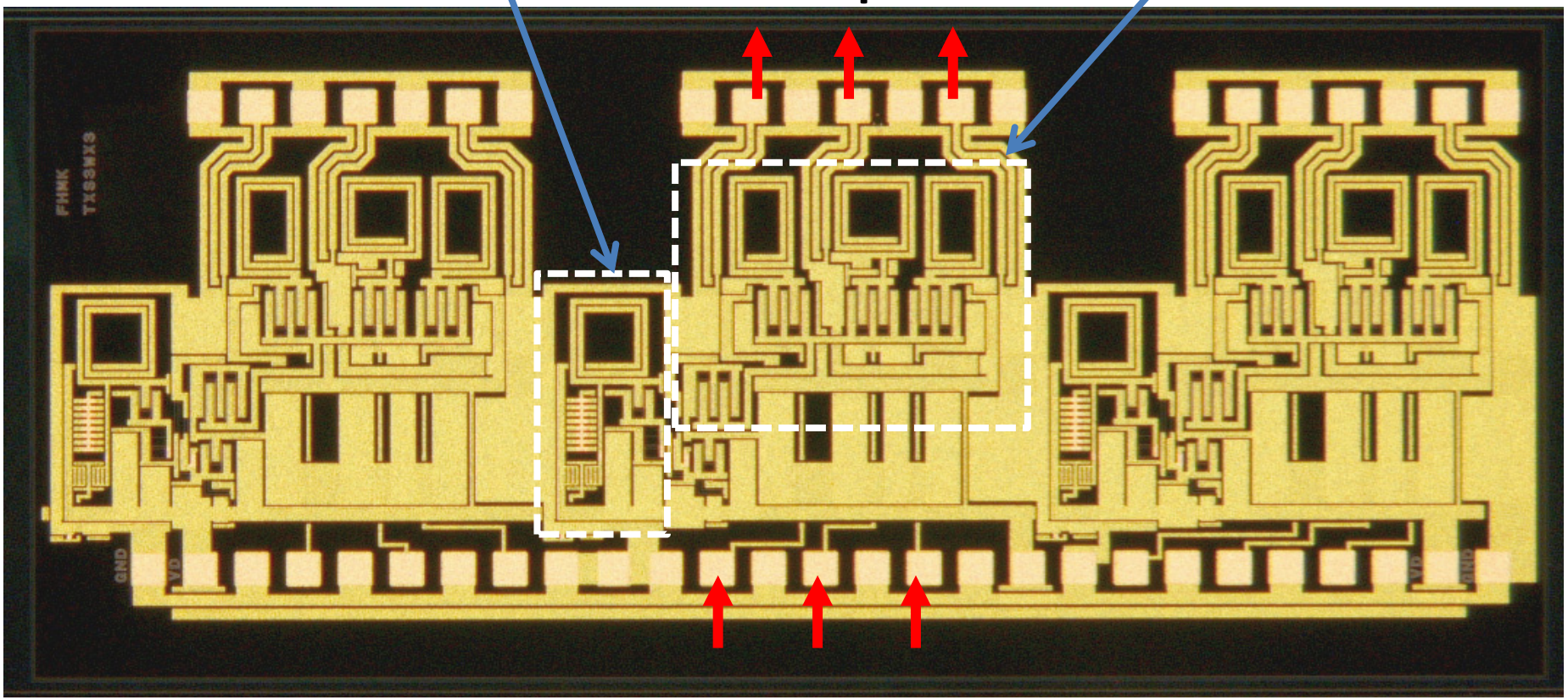


One RF power
source

GaN Gate Drive RF Transmitter for 9 Outputs

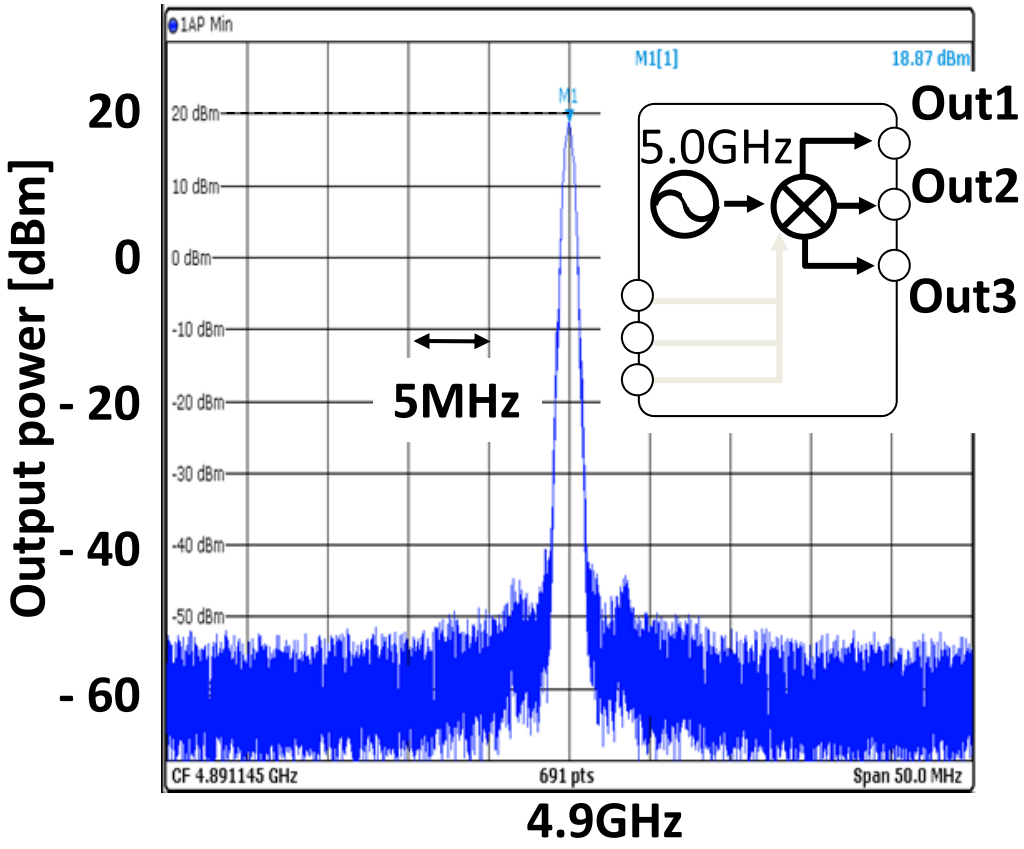


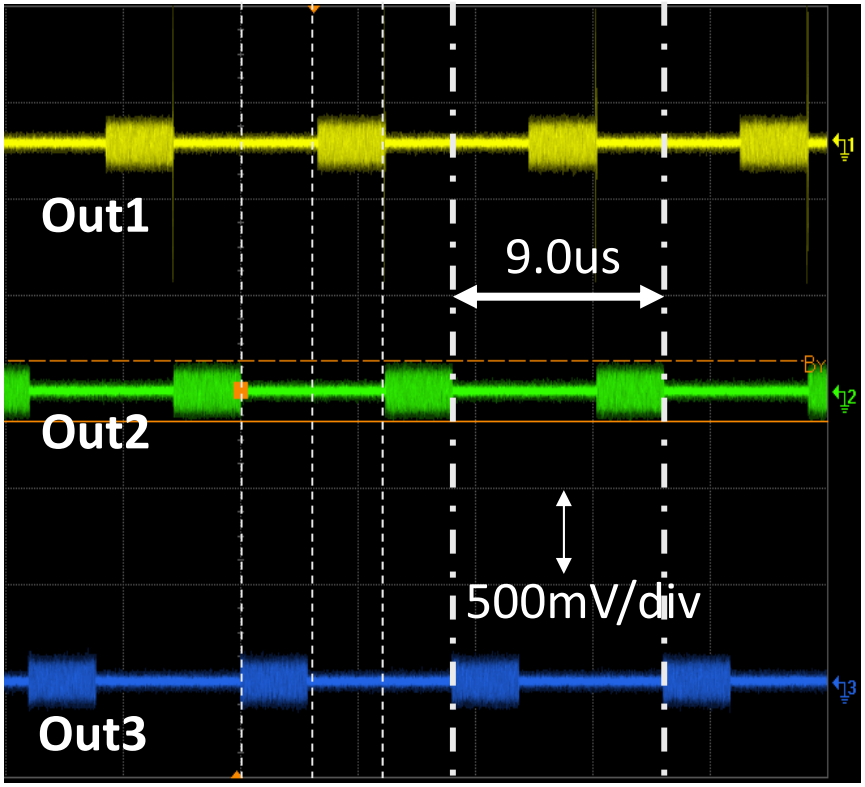
Compact GaN/Si Gate Drive RF Transmitter



- Power Consumption : 1.95 W (13V,150mA)

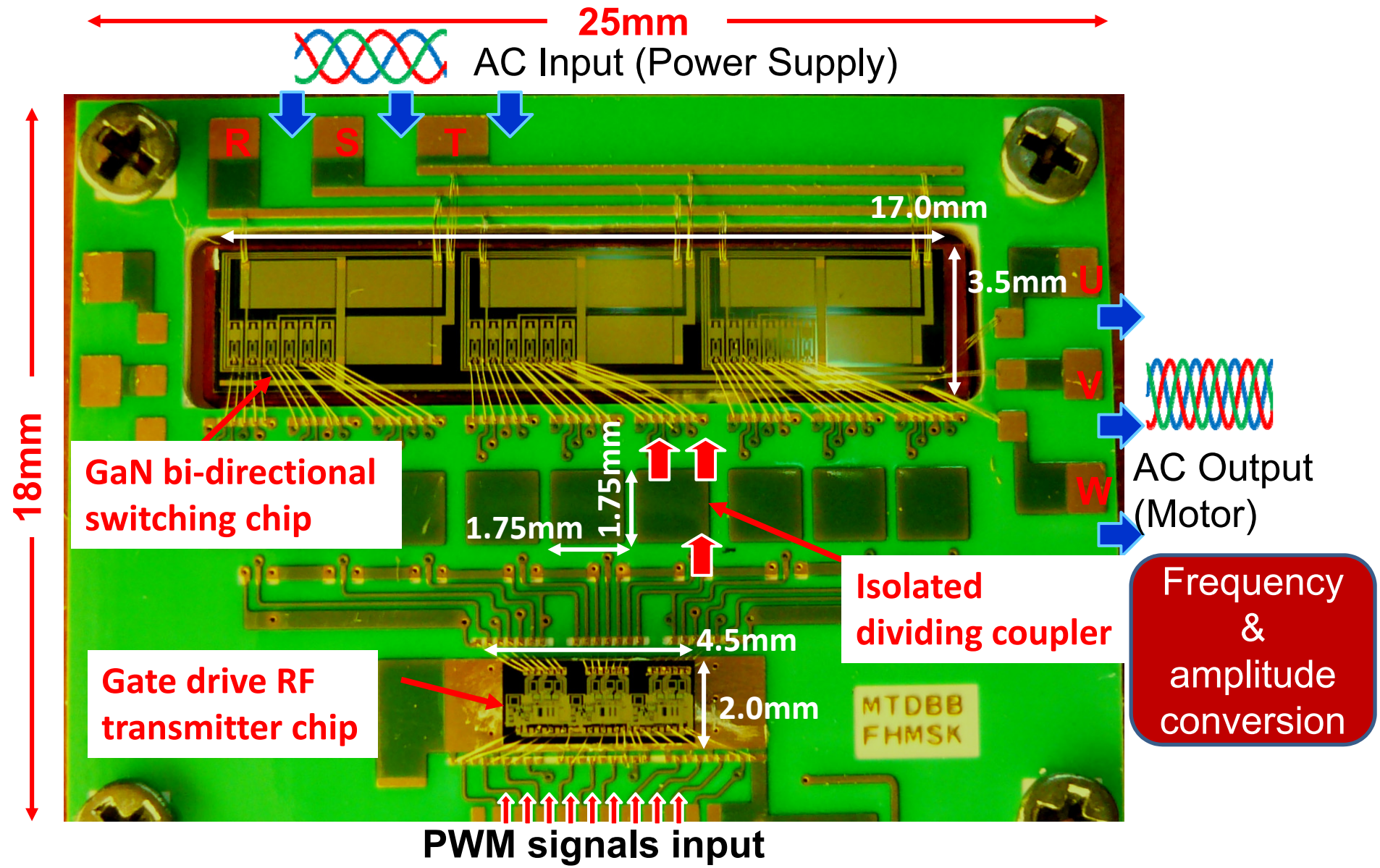
GaN Gate Drive RF Transmitter



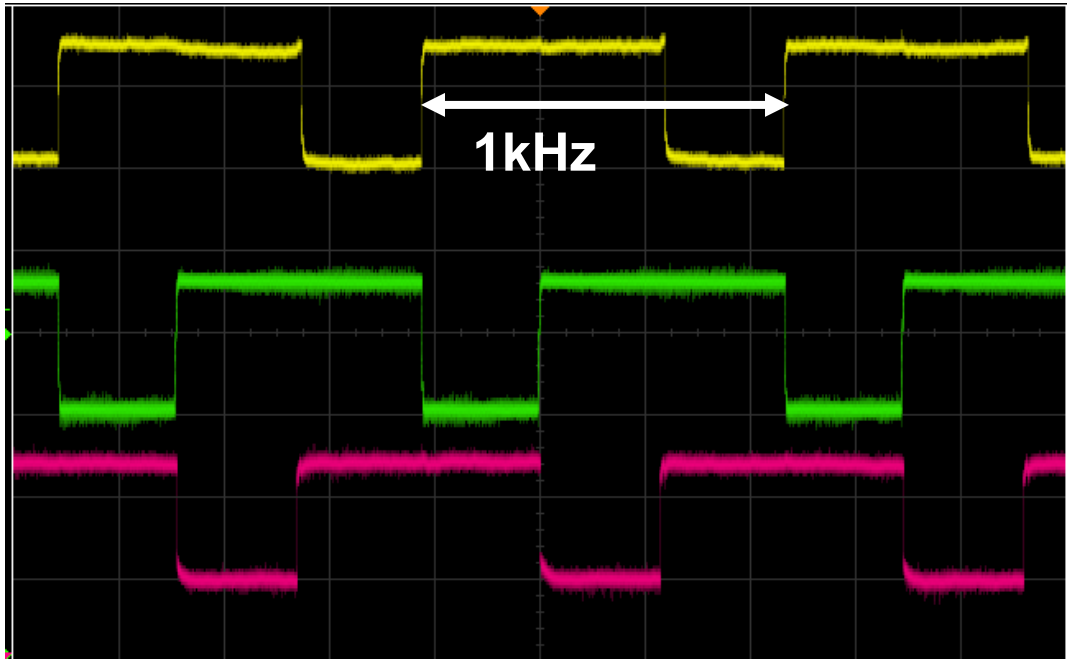


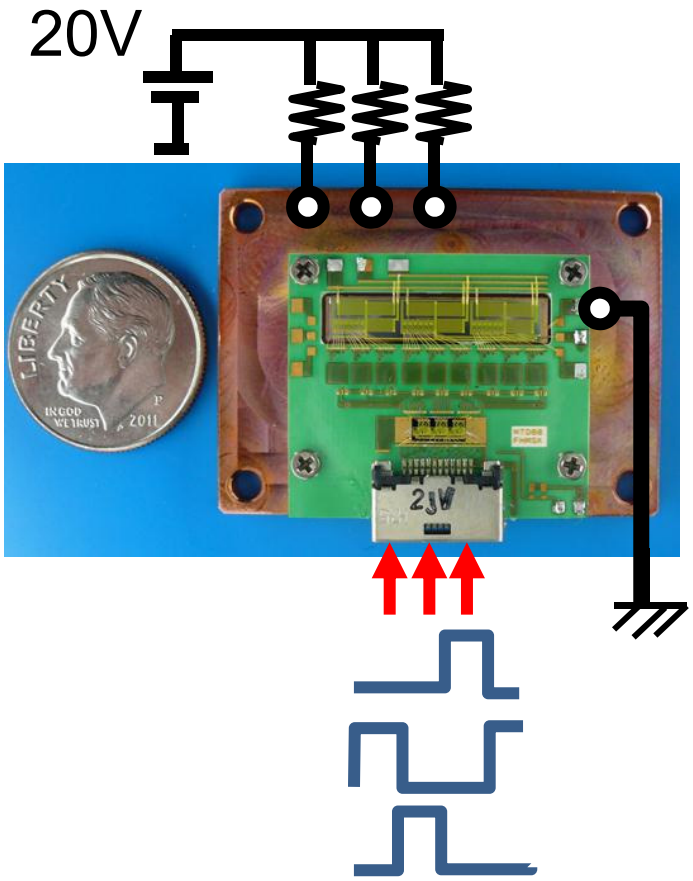
- 20 dBm output
- Sequence output operation

Compact 3x3 Matrix Converter for 5kW



Evaluation of 3x3 Matrix Converter

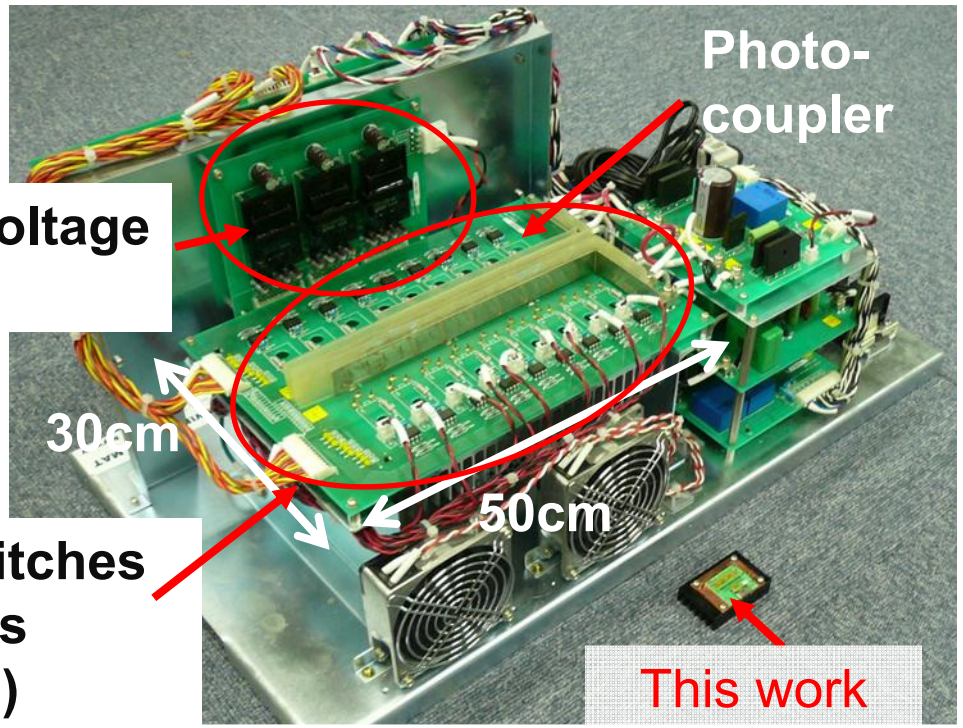


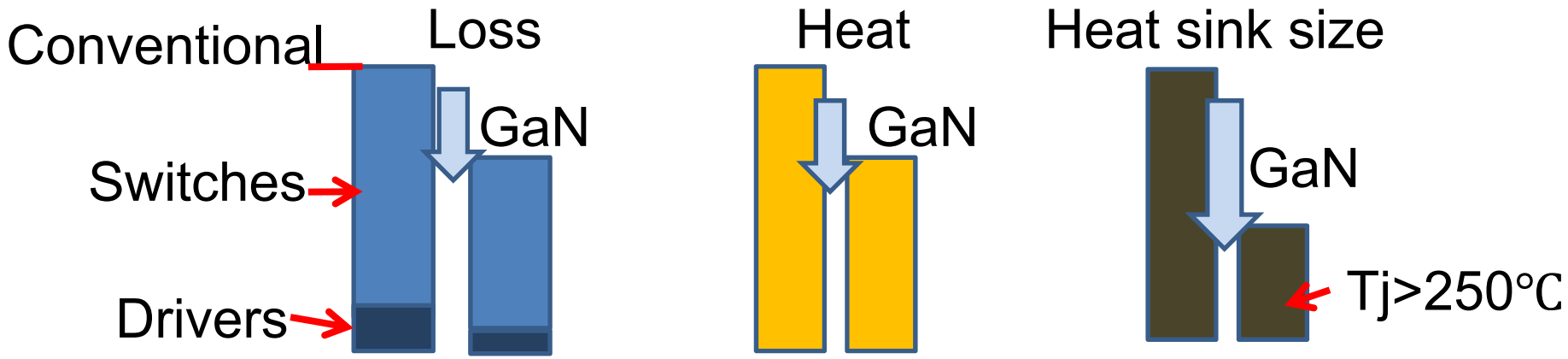


- Achieved switching operation

Size Comparison

Size Reduction
: Less than 1/100





Conclusion

Ultra Compact 5kW 3x3 Matrix-convertor

- A 3x3 RF triggered GaN bi-directional switching chip
- Isolated dividing couplers in a P.C.B
- A gate drive RF transmitter chip

Achieved Sequence Switching Operation

An Electromagnetic Clip Connector for In-Vehicle LAN to Reduce Wire Harness Weight by 30%

Atsutake Kosuge, Shu Ishizuka, Lechang Liu, Akira Okada, Masao Taguchi, Hiroki Ishikuro, and Tadahiro Kuroda

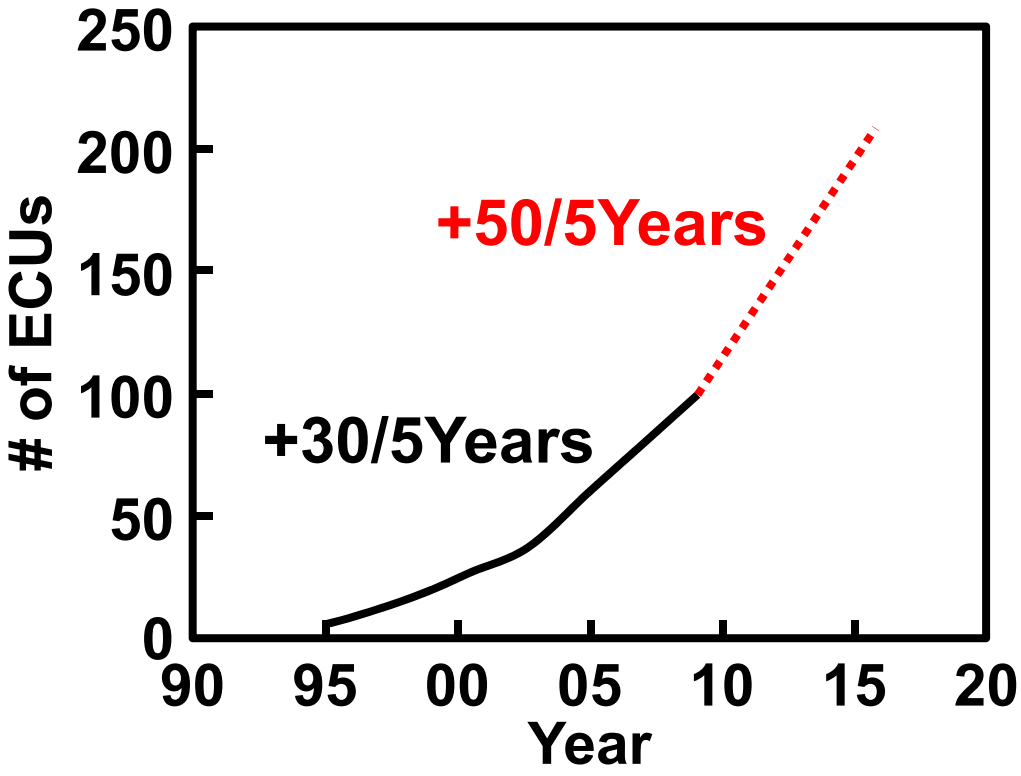
Keio University, Yokohama, Japan

Outline

- Background
- Electromagnetic Clip Connector (EM-Clip)
  - In-Vehicle LAN with EM-Clip
  - Bi-Directional Transmission Line Coupler
- EMI and EMS Tolerant Transceiver
  - *N*-x Manchester Encoding
  - Correlator Based Clock Recovery
- Measurement Results
- Conclusion

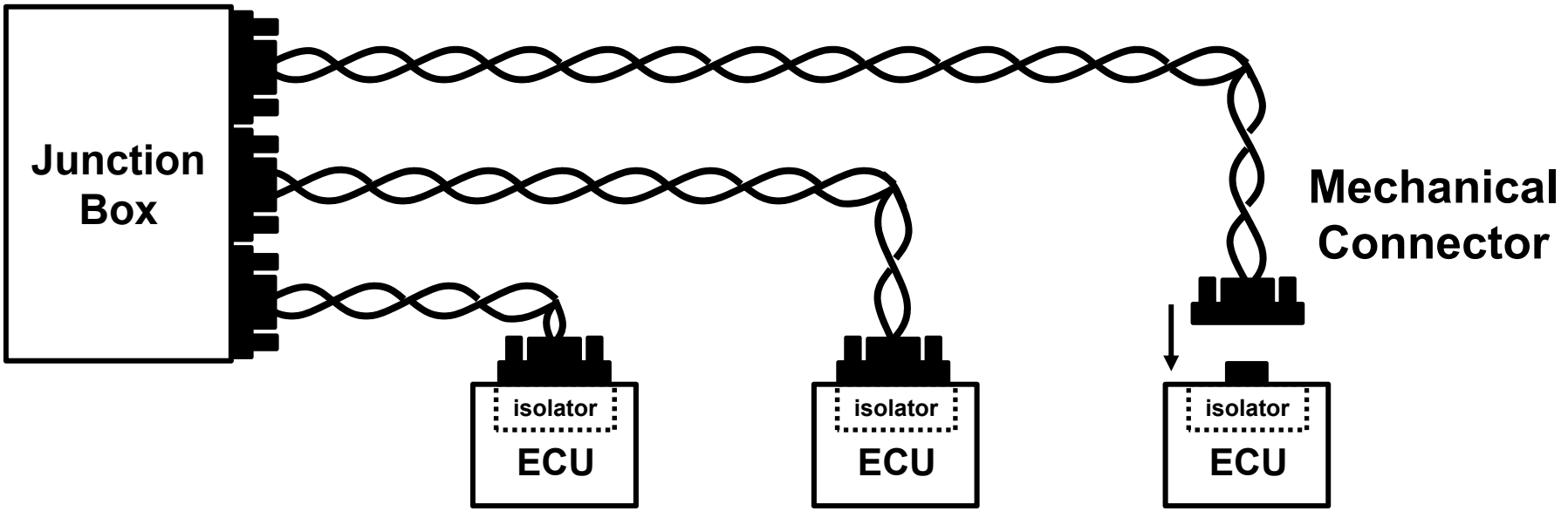
Background

- The number of Electrical Control Unit (ECU) is increasing.
- The weight of wires also increases sharply.
  - The same level with 1 passenger.
- ***Increasing weight decreases fuel efficiency.***



Issues of Conventional In-Vehicle LAN

- Connectors with heavy protection against vibration
- Junction box to stabilize connectors
- Wires to take detour for Junction box

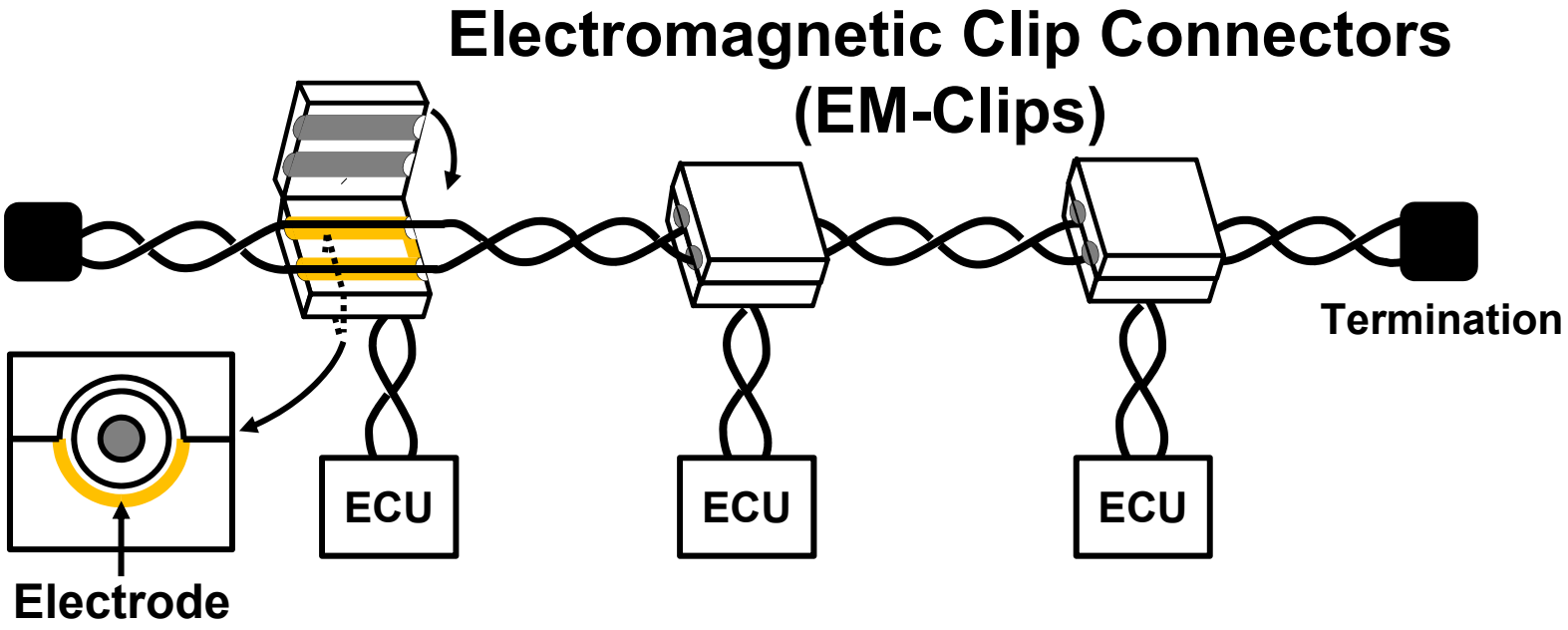


Outline

- Background
- **Electromagnetic Clip Connector (EM-Clip)**
  - **In-Vehicle LAN with EM-Clip**
  - **Bi-Directional Transmission Line Coupler**
- EMI and EMS Tolerant Transceiver
  - *N*-x Manchester Encoding
  - Correlator Based Clock Recovery
- Measurement Results
- Conclusion

In-Vehicle LAN with EM-Clip

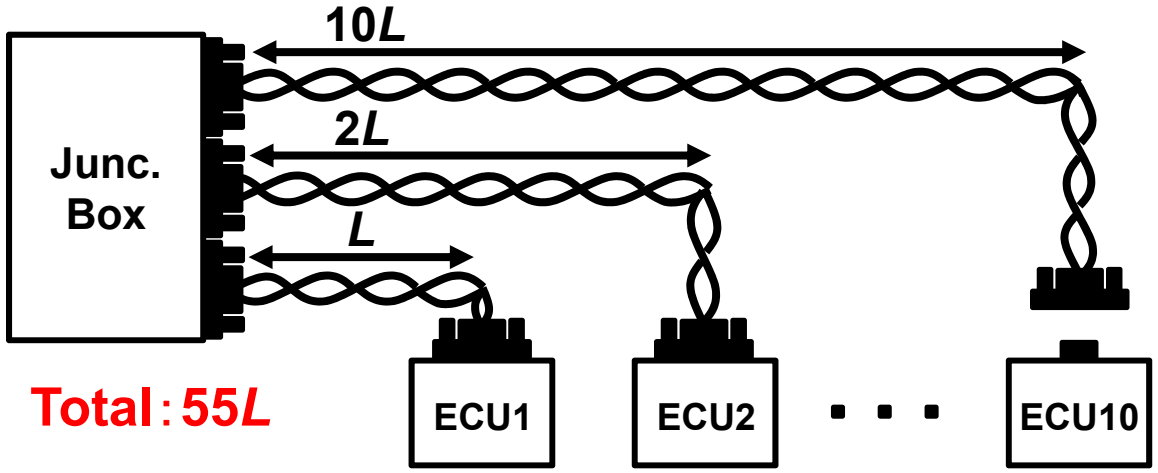
- Clip-like connection
- Strong vibration tolerance
  - No need for heavy protection and Junction box
  - No detouring



Effects of EM-Clip

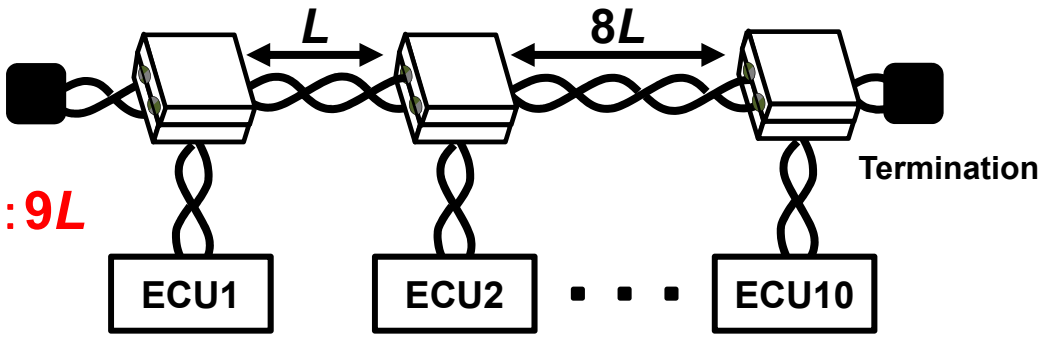
- ***Reducing Wire Harness Weight by 30%***
  - Improving the fuel efficiency by 2%

- Wire Harness Weight
  - Power Lines: 50%
  - Sig. Lines:35%
  - Connector:10%



(a) Conventional In-Vehicle LAN according to Flexray standard.

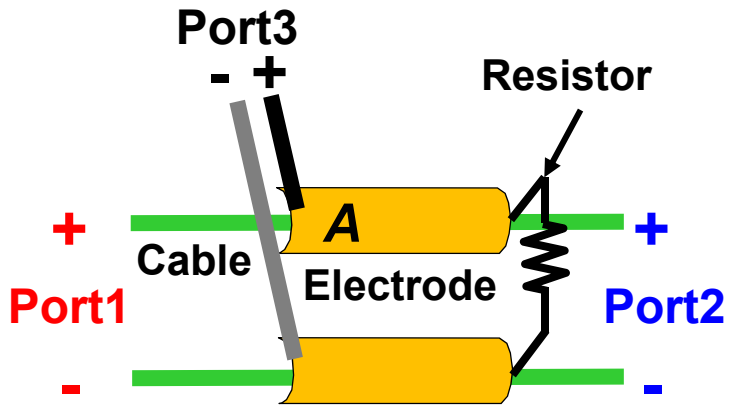
- By using EM-Clips
  - >80% signal lines reduced
  - >50% sig. connector reduced
  - Simplify the Junc. Box



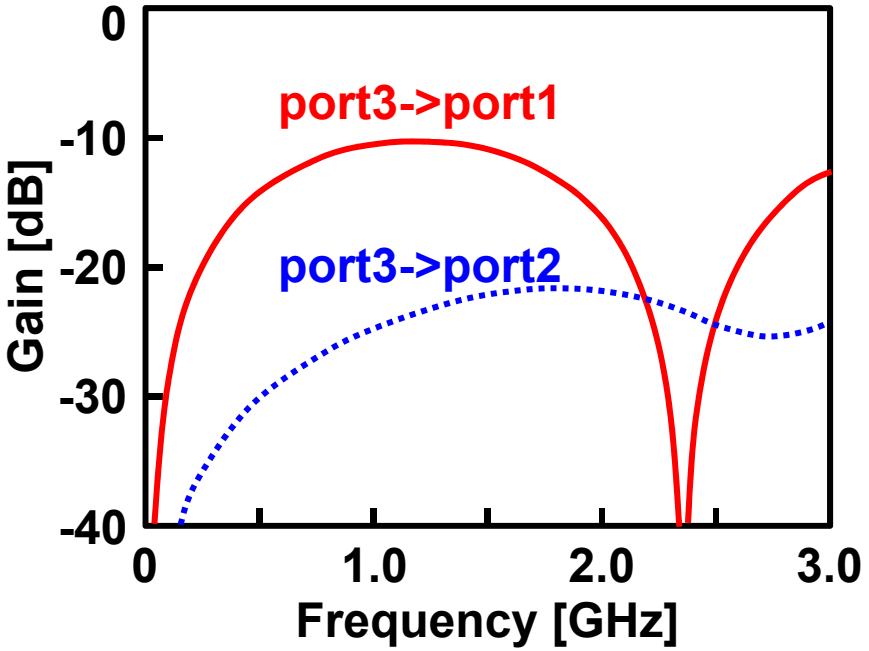
(b) Proposed In-Vehicle LAN using EM-Clips according to Flexray.

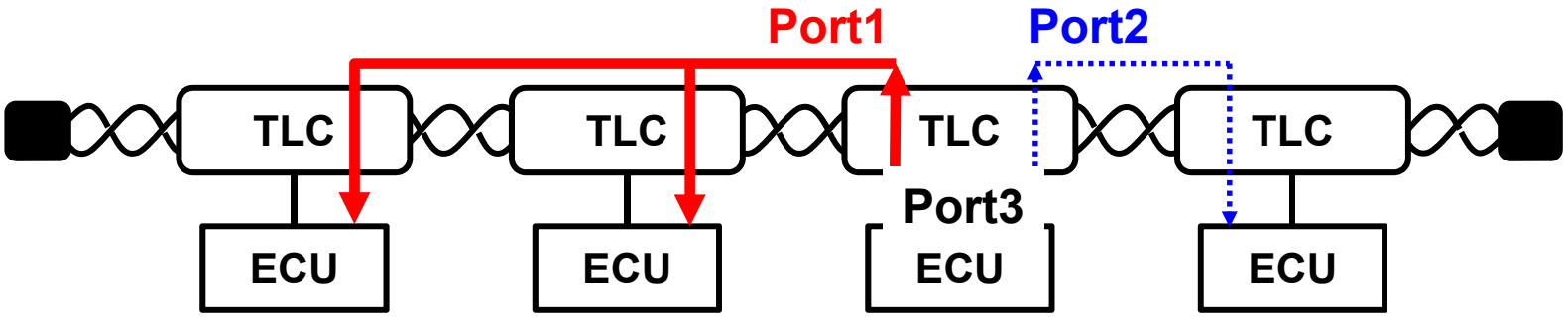
Conventional Transmission Line Coupler (TLC)

- Signals go only in 1 direction (Port3 -> Port1).
  - Signals couple at only 1 point, *A*.



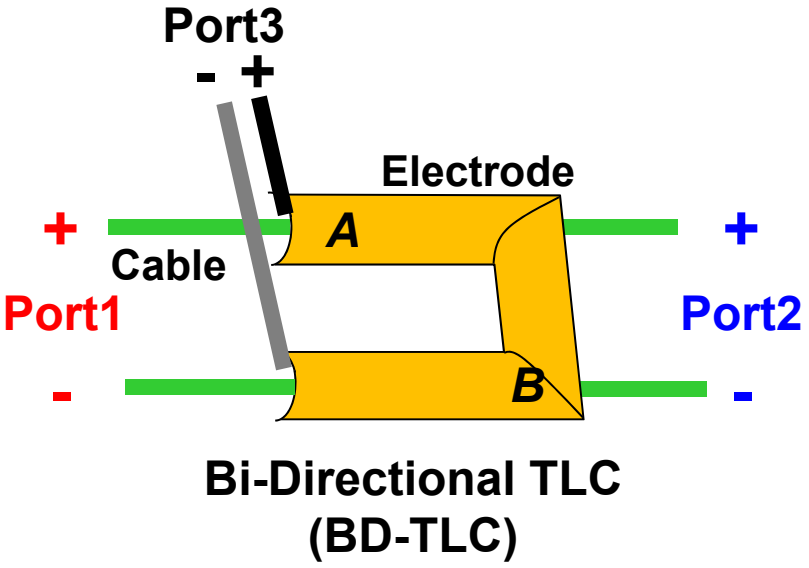
Conventional
Transmission Line Coupler (TLC)



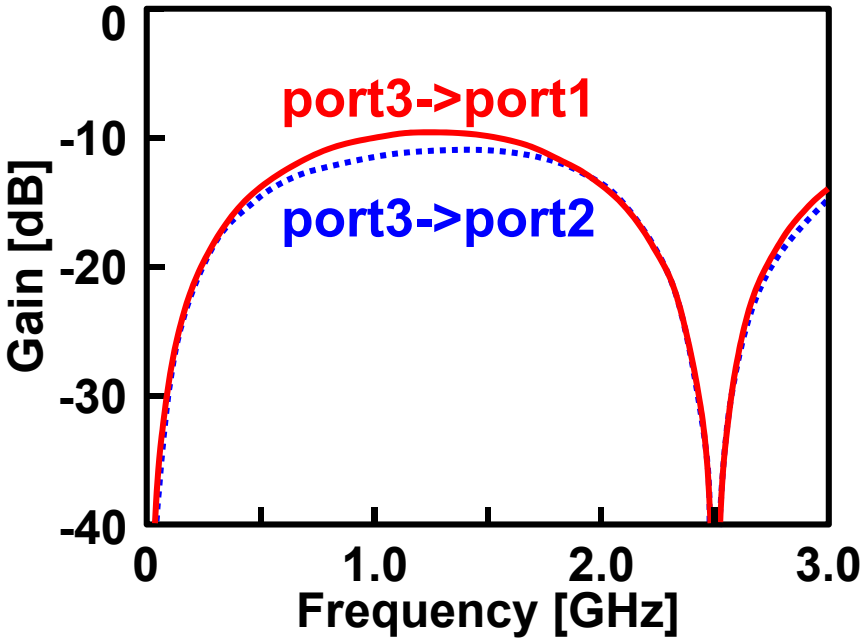


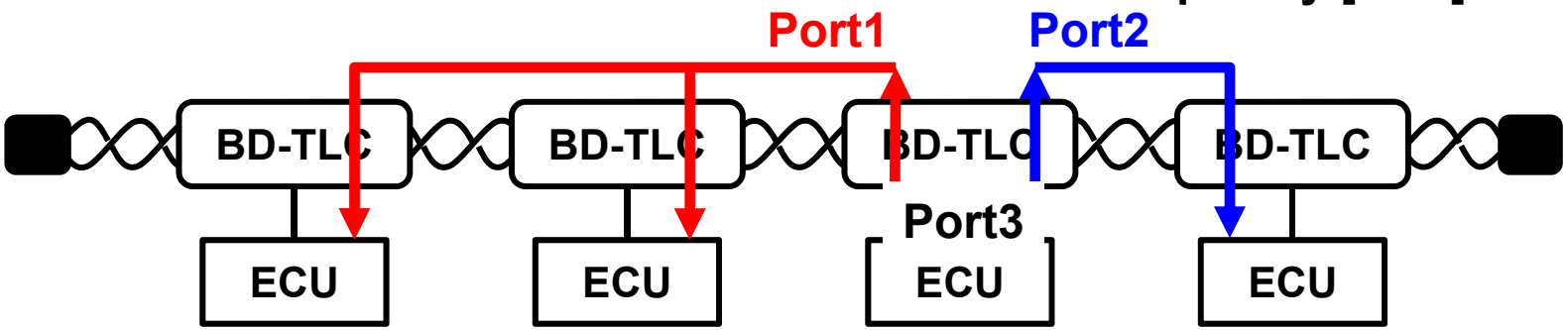
Bi-Directional TLC for EM-Clip

- Signals go in 2 directions (Port3 -> Port1,2).
  - Signals couple at 2 points, *A* and *B*



Bi-Directional TLC
(BD-TLC)



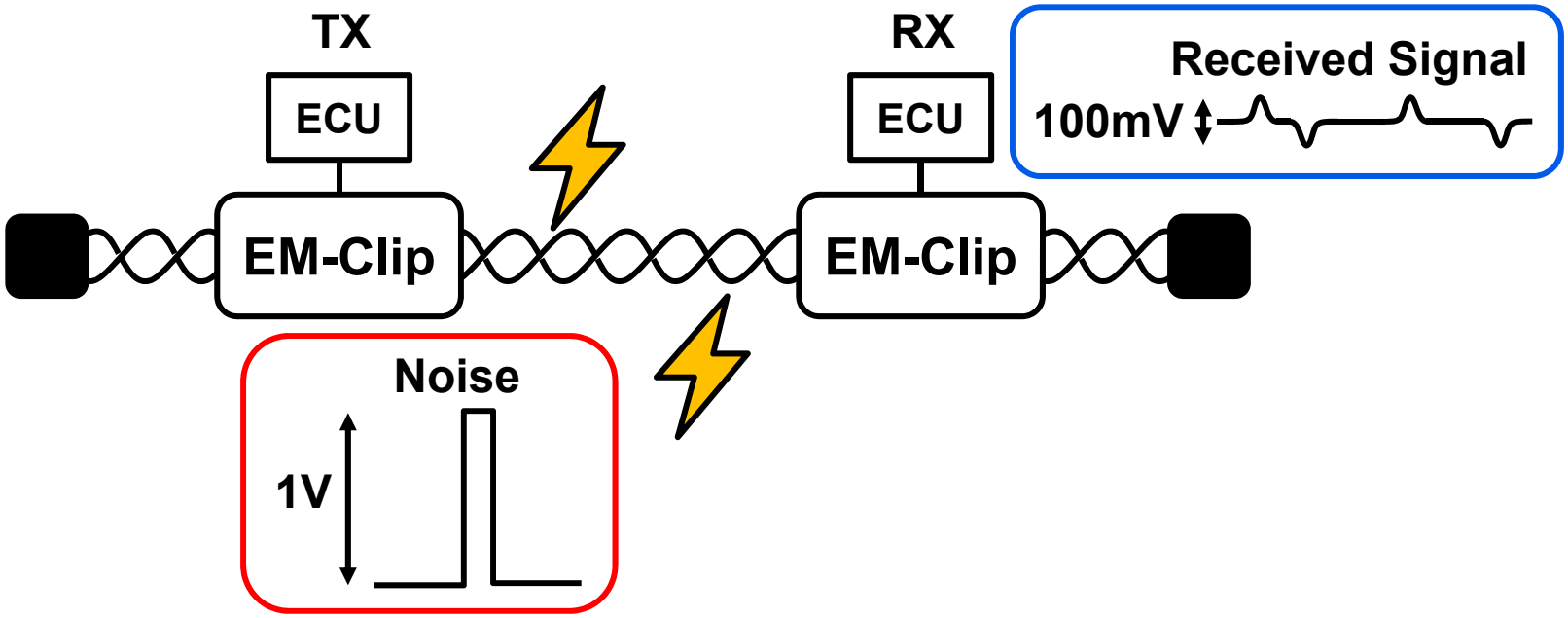


Outline

- Background
- Electromagnetic Clip Connector (EM-Clip)
  - In-Vehicle LAN with EM-Clip
  - Bi-Directional Transmission Line Coupler
- **EMI and EMS Tolerant Transceiver**
  - ***N*-x Manchester Encoding**
  - **Correlator Based Clock Recovery**
- Measurement Results
- Conclusion

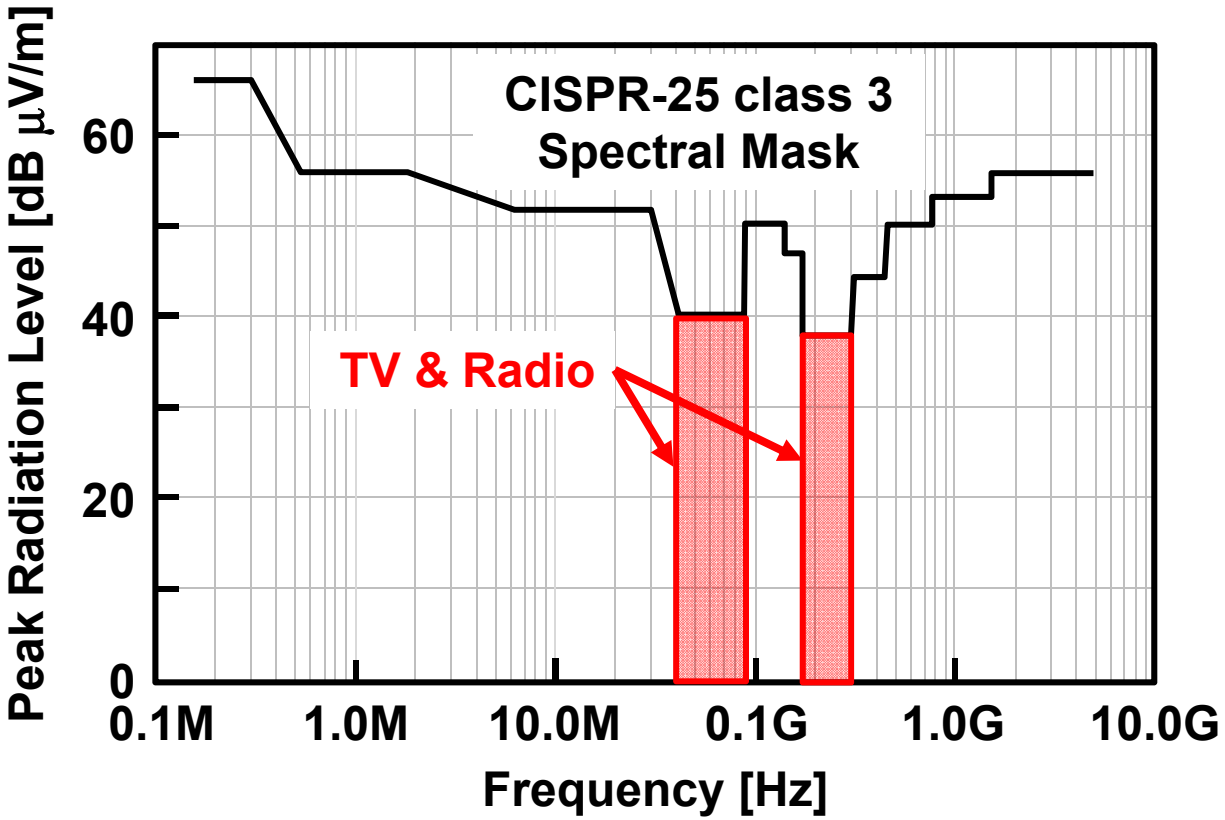
Challenges of In-Vehicle LAN: EMS

- **Large Noise (>1V)**
  - **Under 30dBm 1-400MHz noise environment error-free communication is required.**
- **Small Signal (<100mV)**
  - **Signals need to pass 2 EM-Clips.**



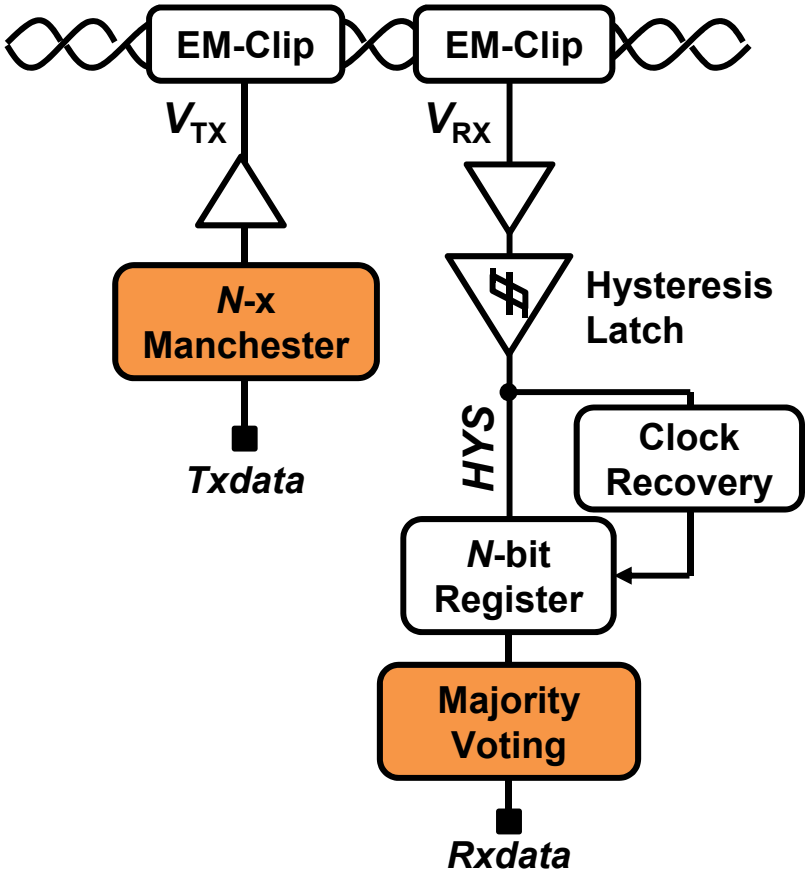
Challenges of In-Vehicle LAN: EMI

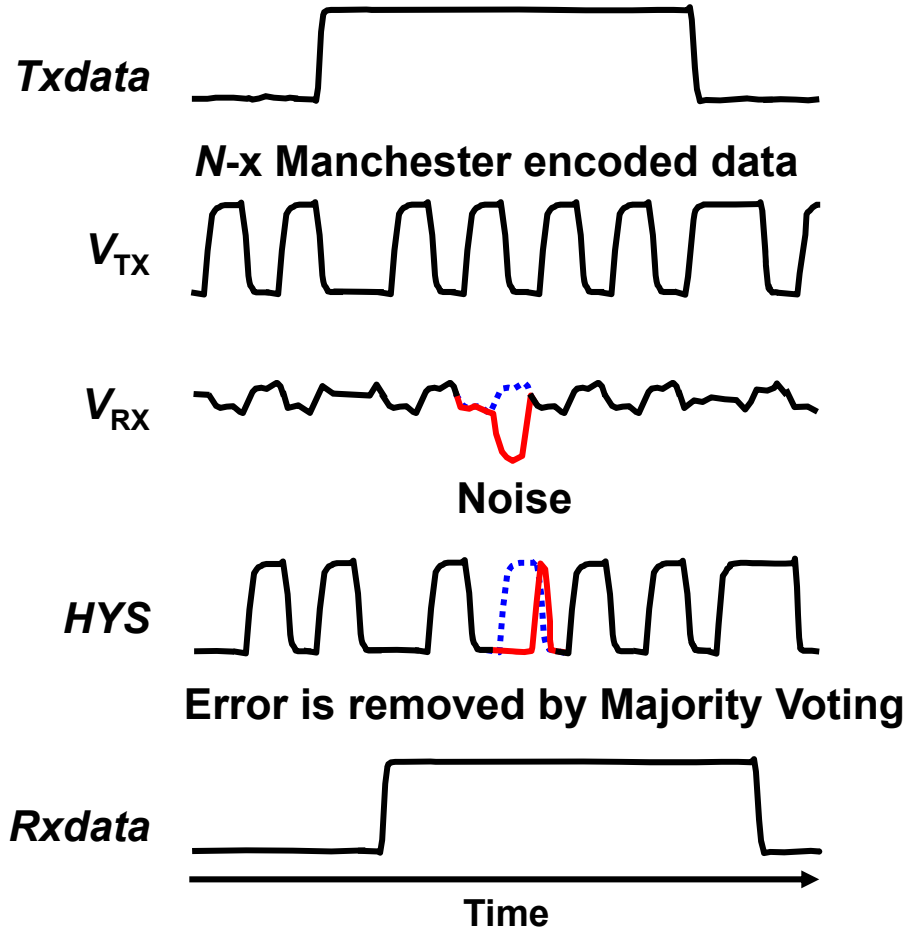
- **Noise radiation <1GHz is strictly regulated.**
  - **TV and Radio band**



FEC by *N*-x Manchester Encoding

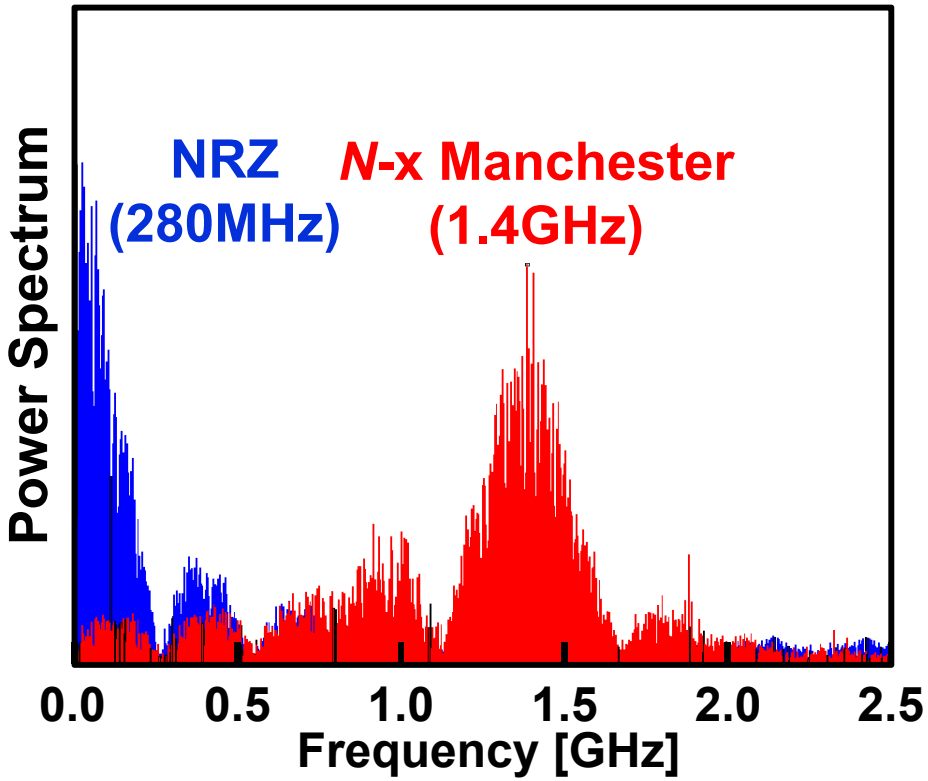
- Transmitted data becomes *N* pulses per a bit.
- Error bits are removed by majority voting.



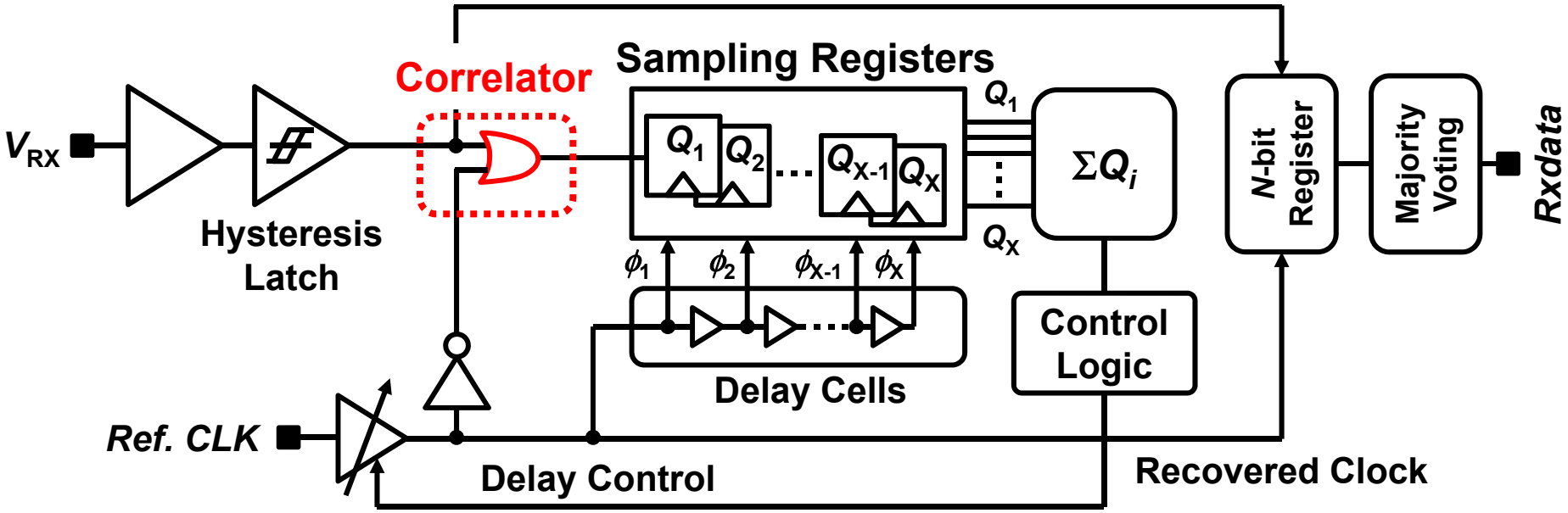


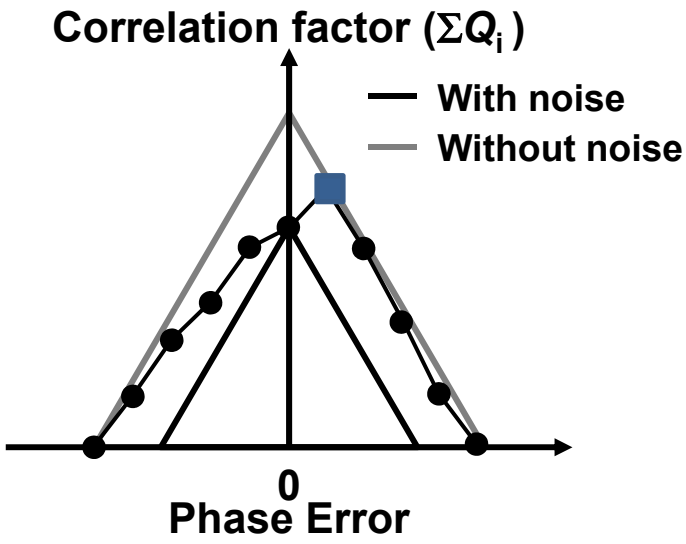
EMI reduction by *N*-x Manchester Encoding

- Up-converted to center around *N*-x clock freq.
- 1.4 GHz for *N*-x freq. to suppress radiations <1GHz
  - *N*=5 results in the data rate of 280Mb/s



Correlator Based Clock Recovery



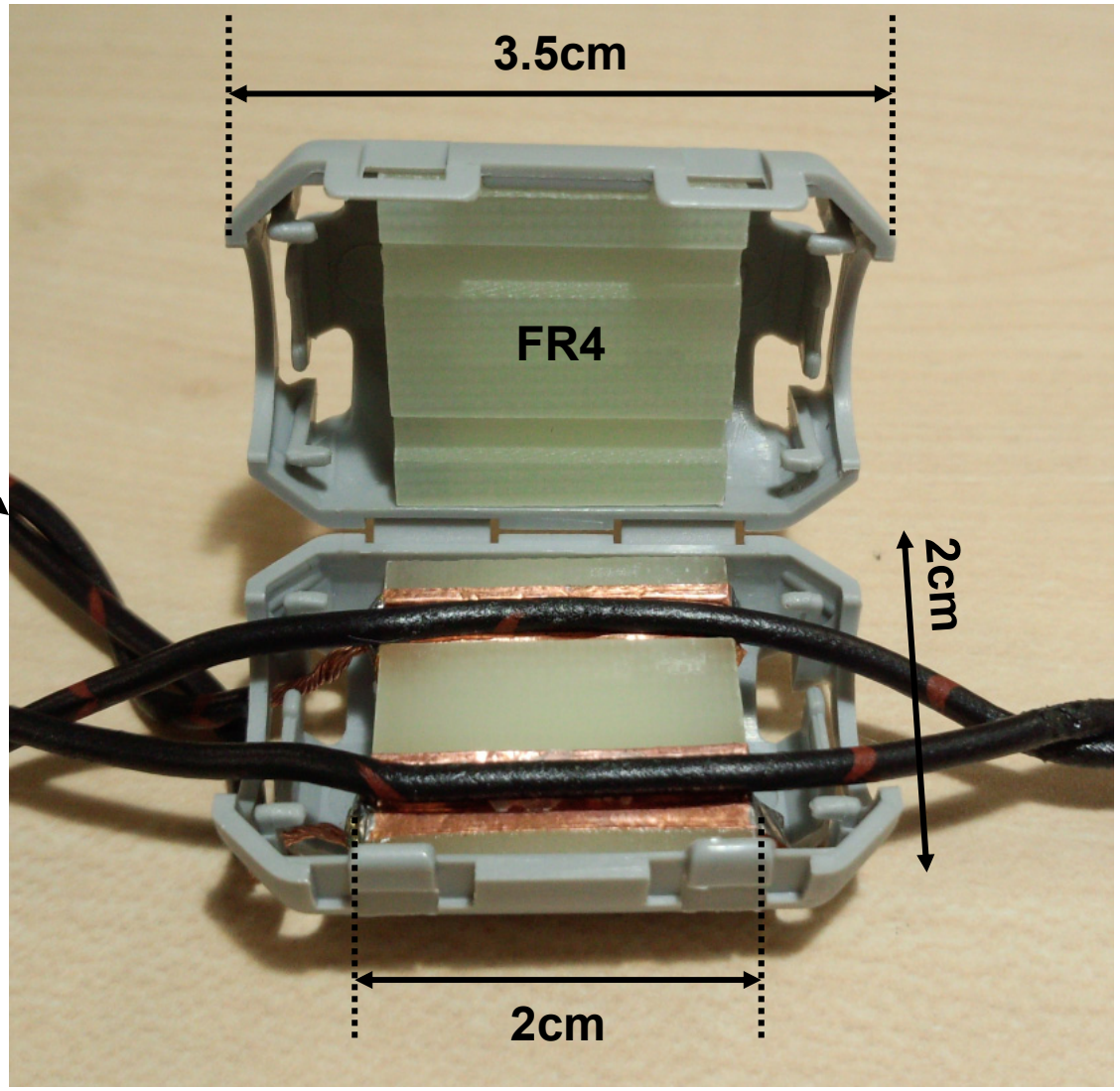


1. Find and store the peak value of ΣQ_i
2. Repeat Step 1
3. Select the highest ΣQ_i
4. Lock the clock

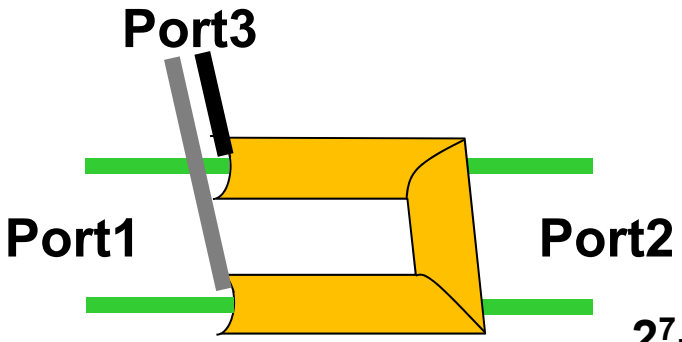
Outline

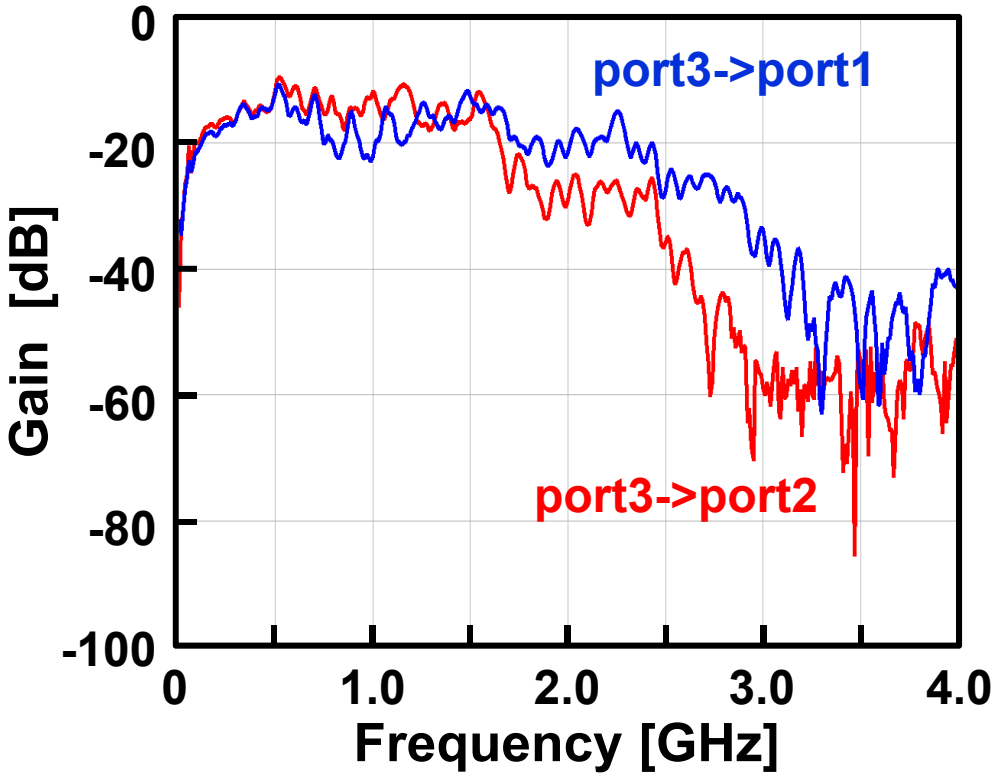
- Background
- Electromagnetic Clip Connector (EM-Clip)
  - In-Vehicle LAN with EM-Clip
  - Bi-Directional Transmission Line Coupler
- EMI and EMS Tolerant Transceiver
  - *N*-x Manchester Encoding
  - Correlator Based Clock Recovery
- **Measurement Results**
- **Conclusion**

Electromagnetic Clip Connector (EM-Clip)

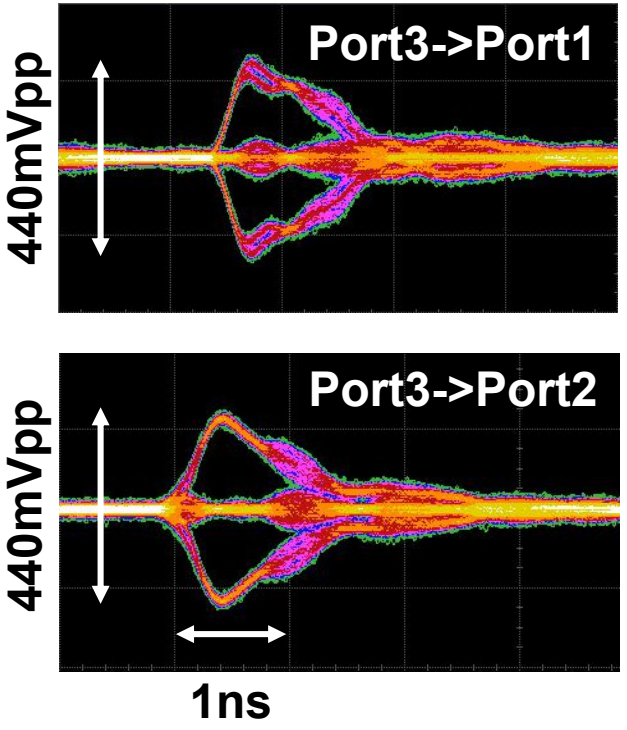


EM-Clip Experimental Results



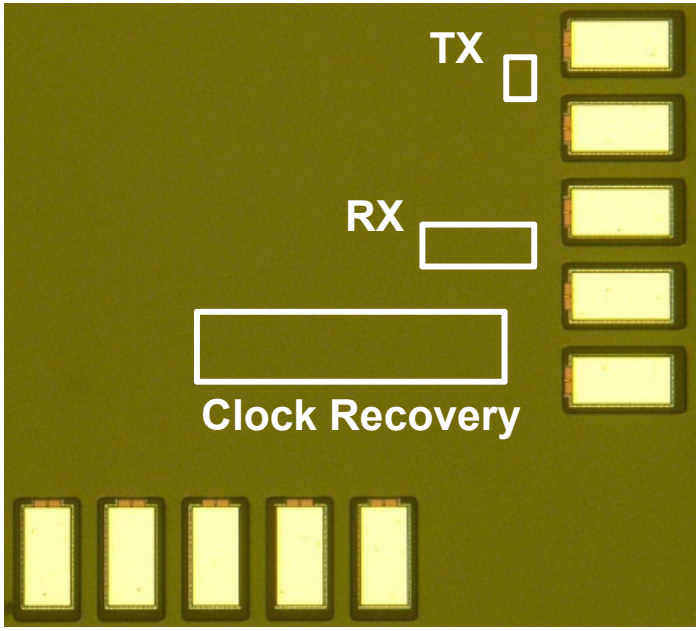


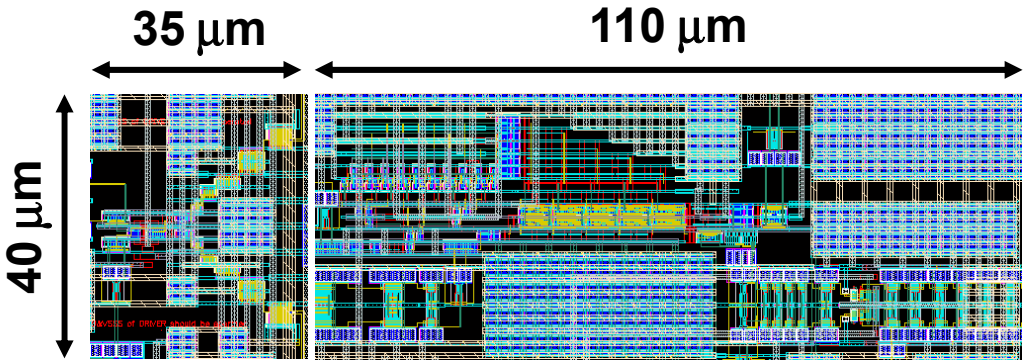
2^7-1 PRBS 280Mb/s

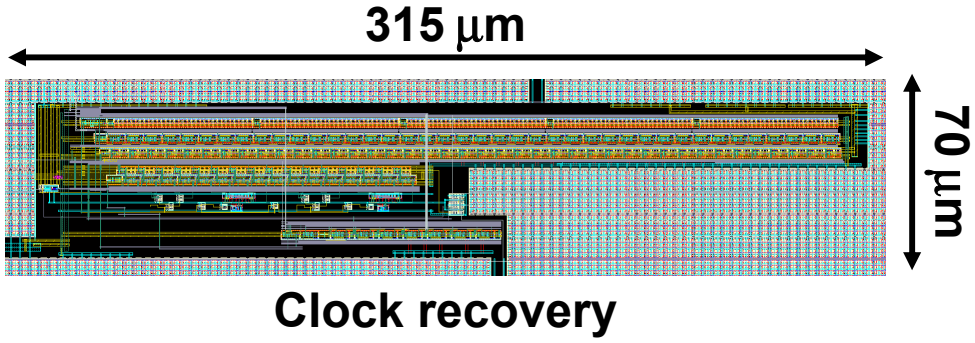


Die Photo

- Implemented in 65nm CMOS

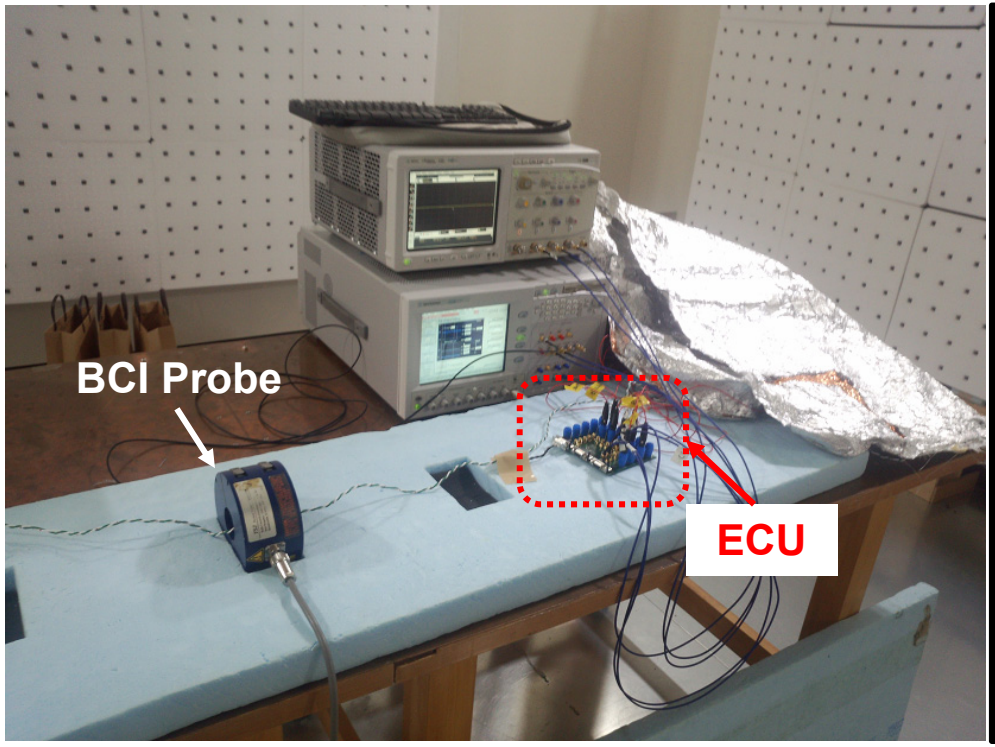




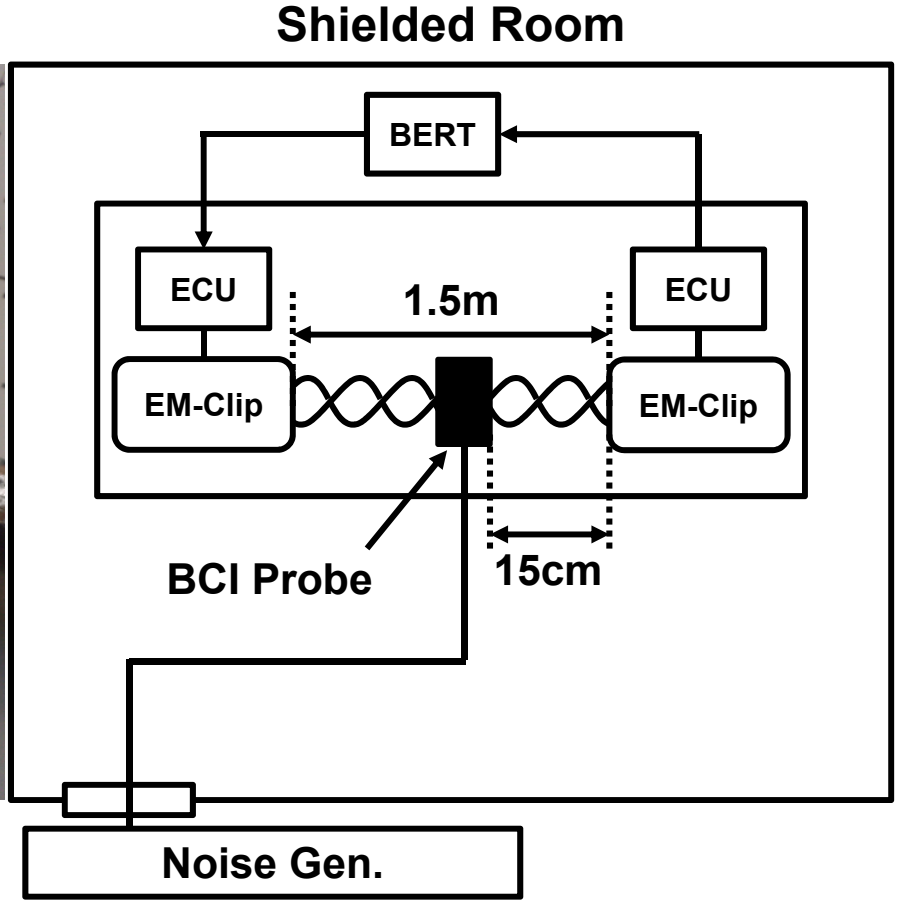


EMS Test Set Up

- BCI method by ISO 11452-4 standard for In-Vehicle LAN noise immunity test



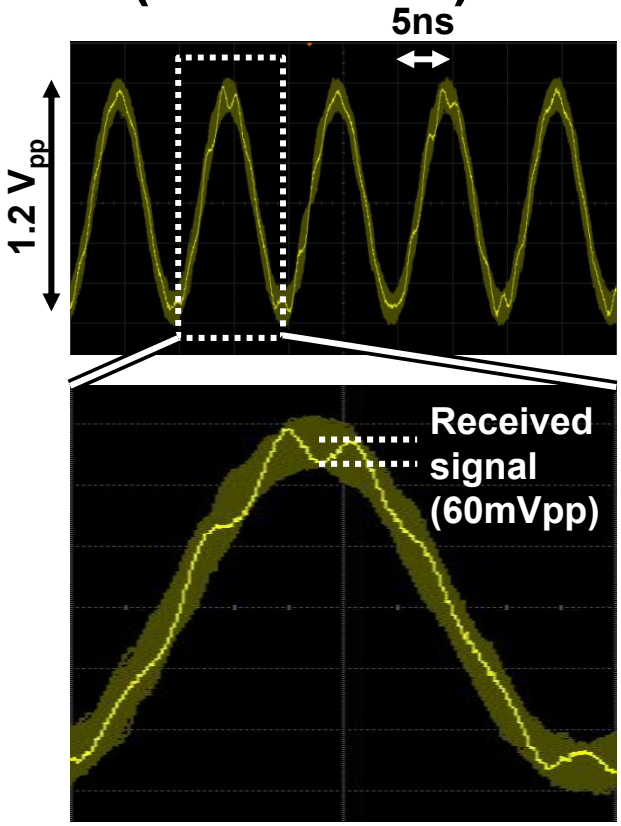
(a) Experimental set up



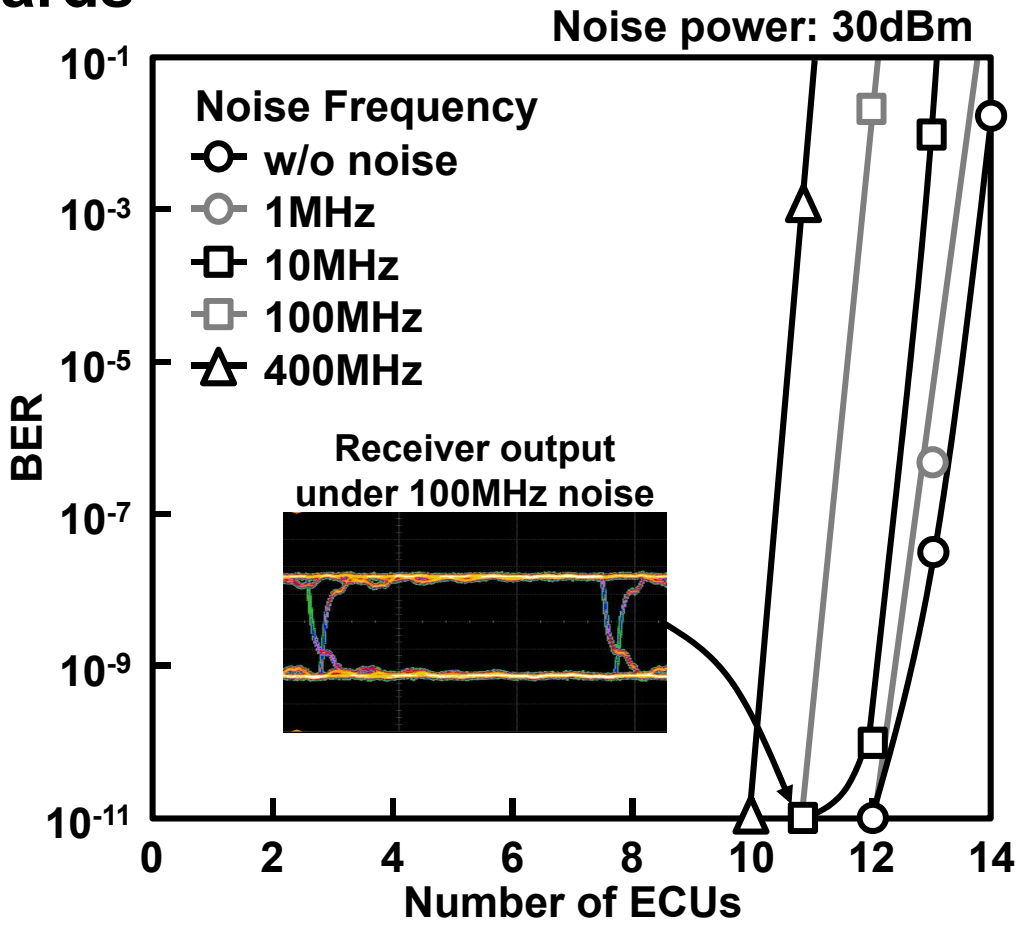
(b) Block diagram

EMS Test Results

- **Error free with 10 ECUs connected**
  - **Satisfied the ISO (Noise immunity) and Flexray (# of ECUs) standards**

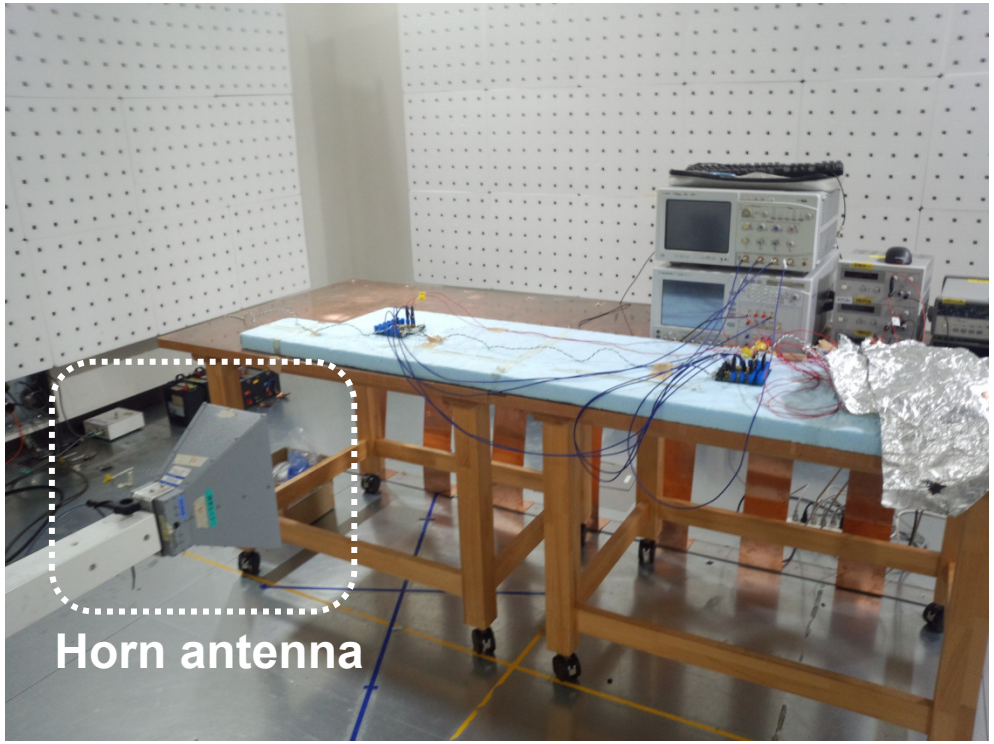


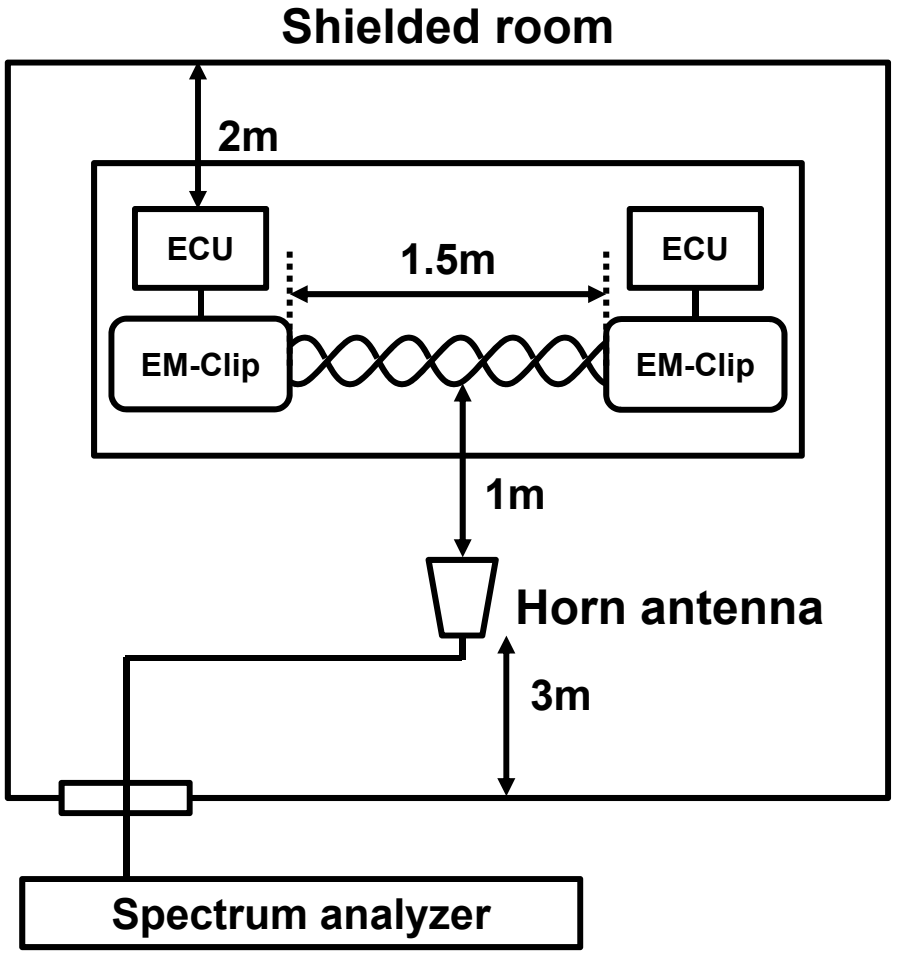
Receiver input under 100MHz noise



EMI Test Set Up

- CISPR standard 25 for In-Vehicle LAN noise radiation test



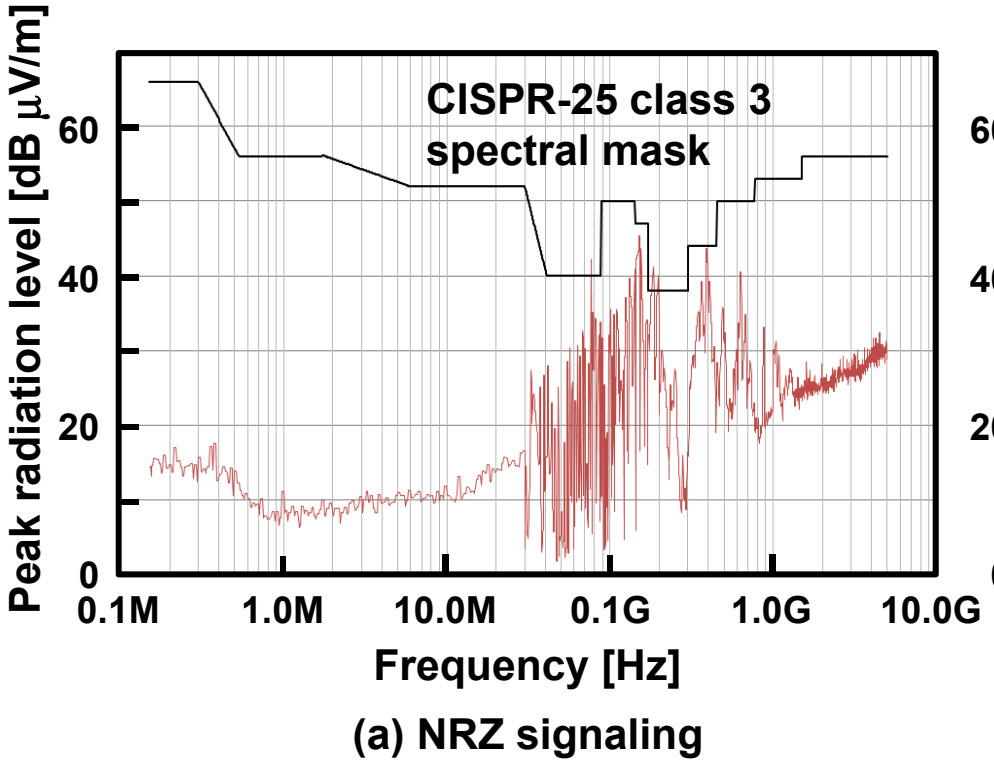


(a) Experimental set up

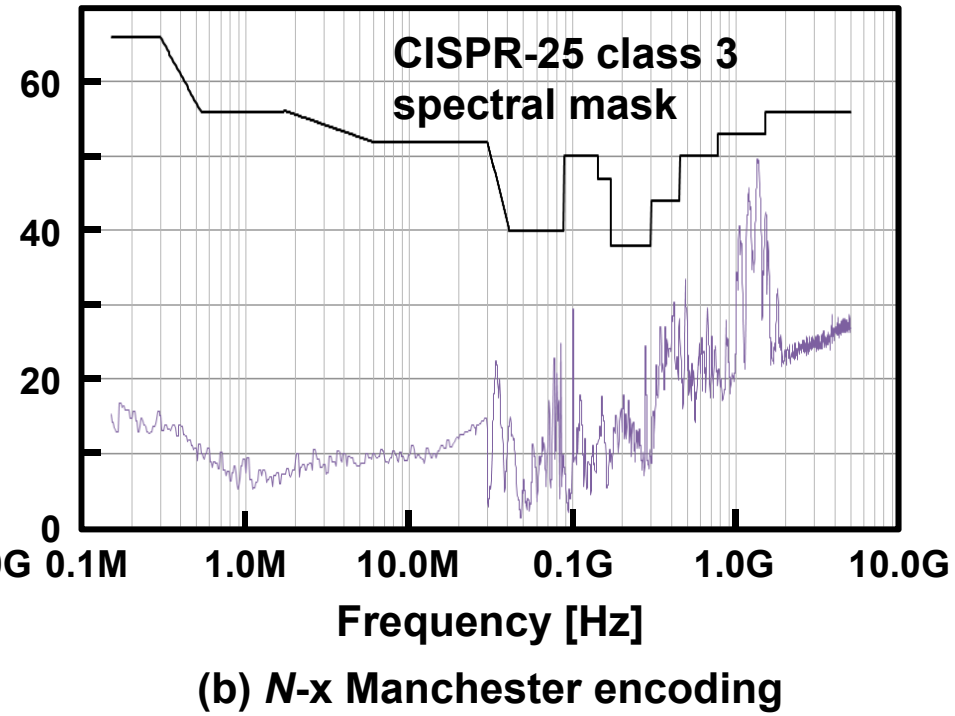
(b) Block diagram

EMI Test Results

- CISPR specification was satisfied.
- Emissions below 1GHz were suppressed.



(a) NRZ signaling



(b) *N*-x Manchester encoding

Conclusion

- Proposed an electromagnetic clip connector (EM-Clip) for In-Vehicle LAN applications
  - Bi-directional TLC for In-Vehicle LAN
  - *N*-x Manchester encoding and correlator based Clock Recovery for EMS and EMI issues
- EM-Clip can reduce the wire harness weight by 30%.
- EMS and EMI specifications are satisfied.

A 60Mb/s Wideband BCC Transceiver with 150pJ/b RX and 30pJ/b TX for Emerging Wearable Applications

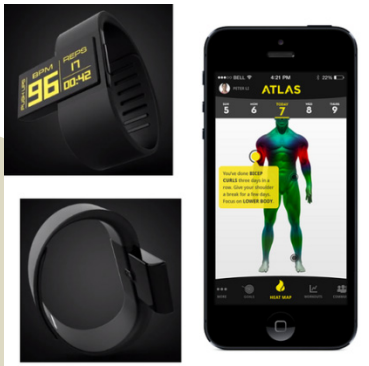
Junghyup Lee[1], Vishal Vinayak Kulkarni[1], Chee Keong Ho[1], Jia Hao Cheong[1], Peng Li[1], Jun Zhou[1], Wei Da Toh[1], Xin Zhang[1], Yuan Gao[1], Kuang Wei Cheng[2], Xin Liu[1], Minkyu Je[1]

[1]Institute of Microelectronics, Singapore
[2]National Cheng Kung University, Tainan, Taiwan

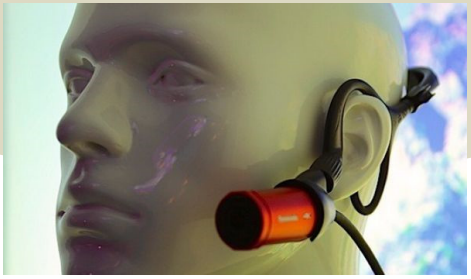
Outline

- Introduction
- Body Channel Characteristics
- Transmitter Design & Architecture
- Receiver Design & Architecture
- Measurement Results
- Summary

Motivation

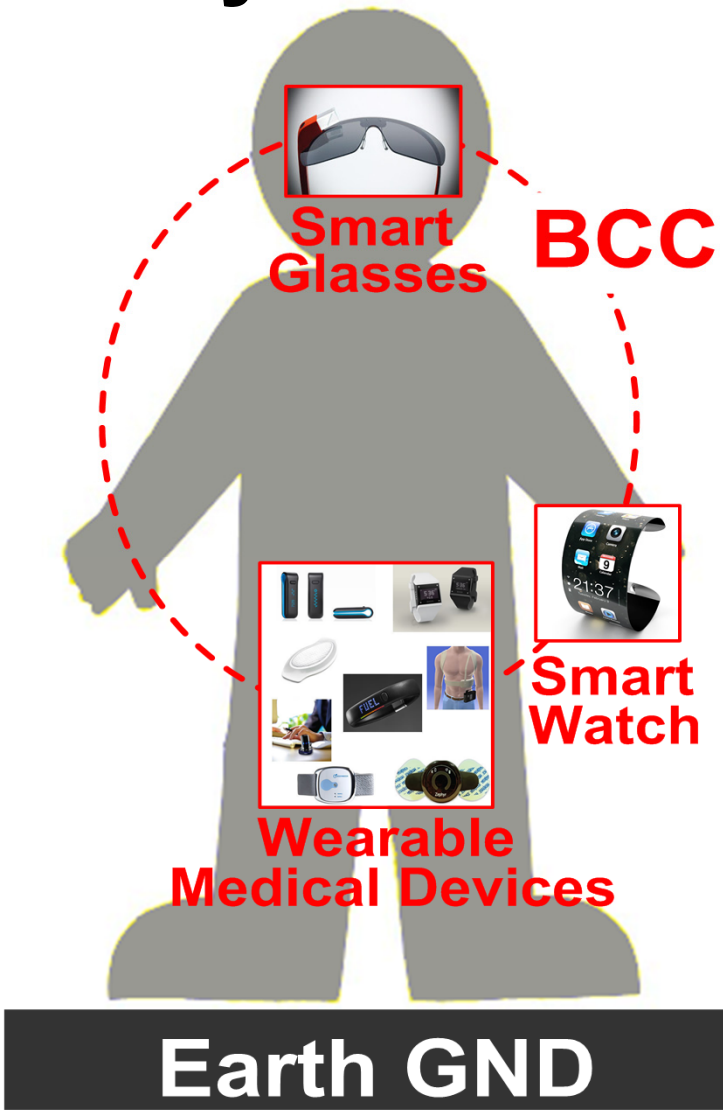


2014 International CES®



Wearable technology is this year's top trend.

Body Channel Communication (BCC)



- **Why BCC rather than air-channel?**
  - **A significant reduction of power consumption**
  - **No bulky antennas**
  - **No fading effect**
- **Key requirements**
  - **High data rate**
  - **High energy efficiency**

BCC is an excellent alternative over conventional wireless communication through the air.

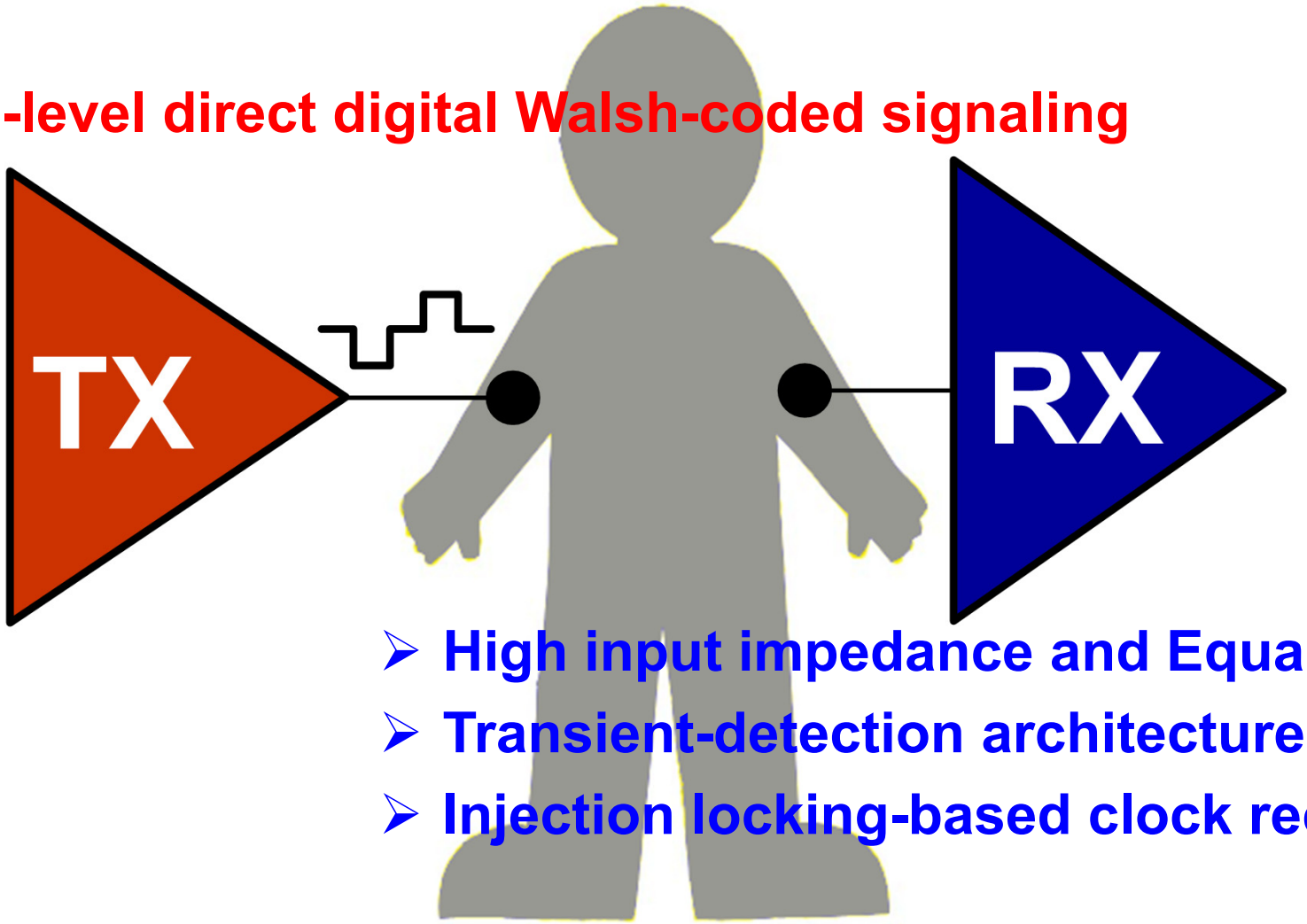
Previous Works

	Song, ISSCC '07	Fazzi, ISSCC '09	Cho, JSSC '09	Bae, JSSC '12
Signaling	Direct Digital		FSK	
Energy/bit of TX	71pJ/b ☺	70pJ/b ☺	240pJ/b ☹	200pJ/b ☹
Energy/bit of RX	189pJ/b ☺	250pJ/b ☹	370pJ/b ☹	240pJ/b ☹
Maximum Data Rate	10Mb/s ☹	8.5Mb/s ☹	10Mb/s ☹	10Mb/s ☹

A highly efficient wideband BCC transceiver is required.

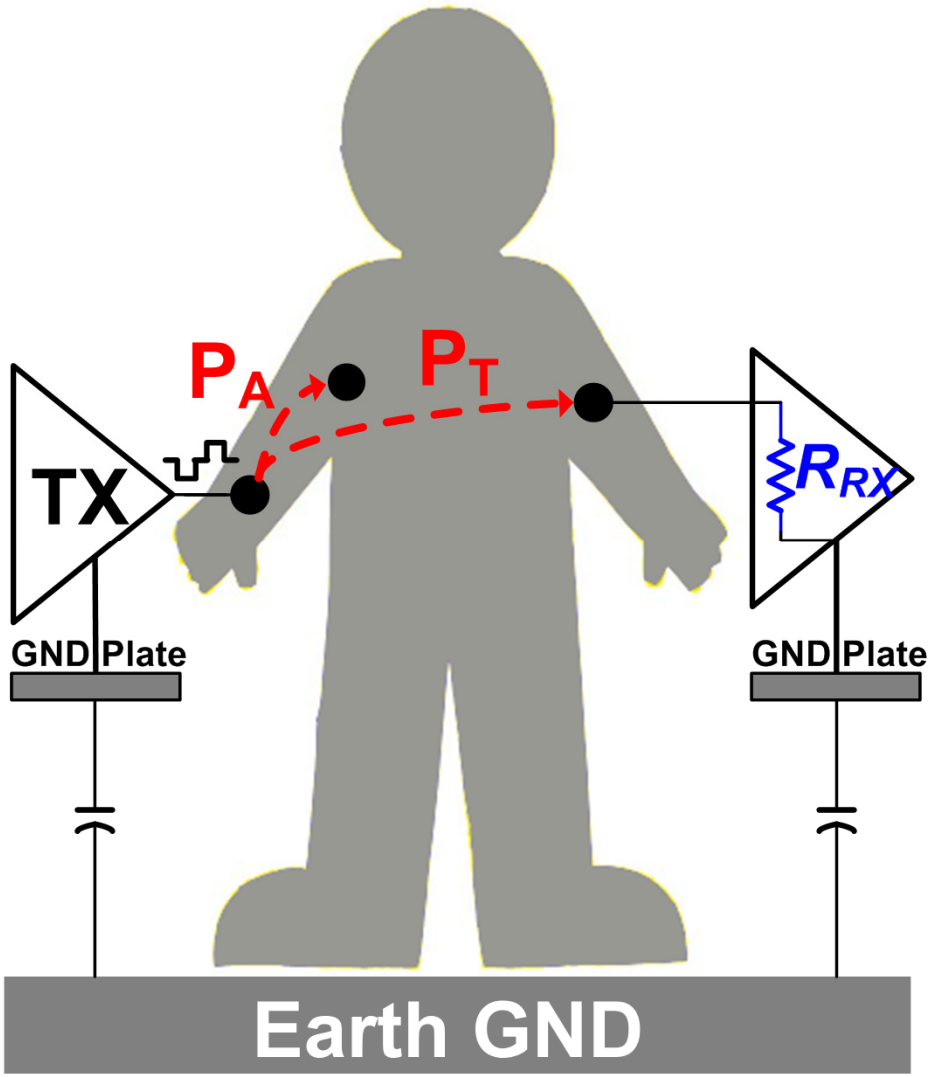
Proposed Key Features

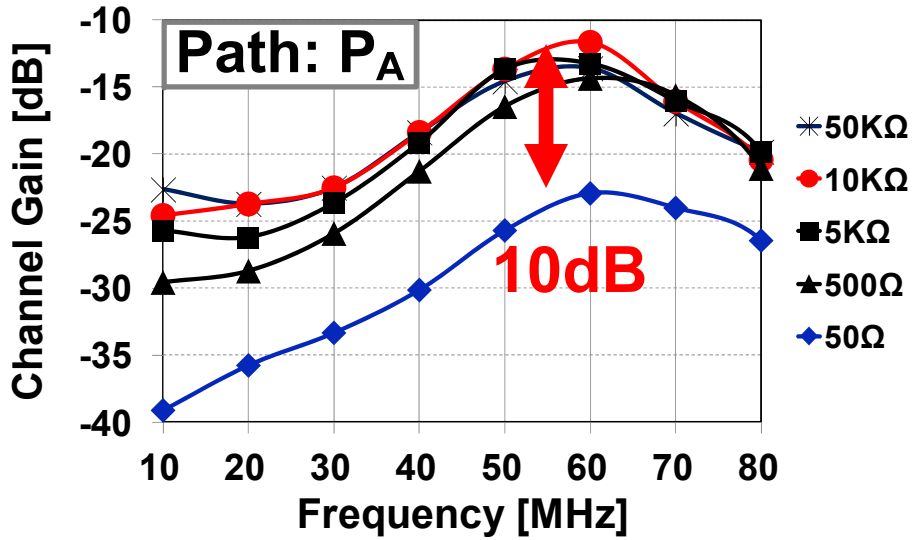
- 3-level direct digital Walsh-coded signaling

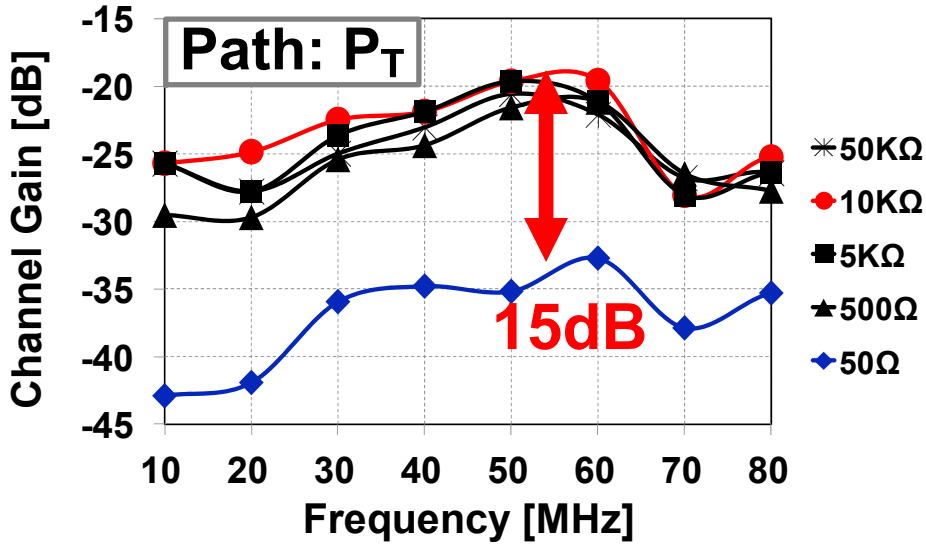


- High input impedance and Equalizer
- Transient-detection architecture
- Injection locking-based clock recovery

Body Channel Characteristics







- Body channel has band-pass characteristics.
- The path loss is improved up to 15dB by high R_{RX}.

Generation of Band-limited TX Output

Clock = 160MHz

Input Data

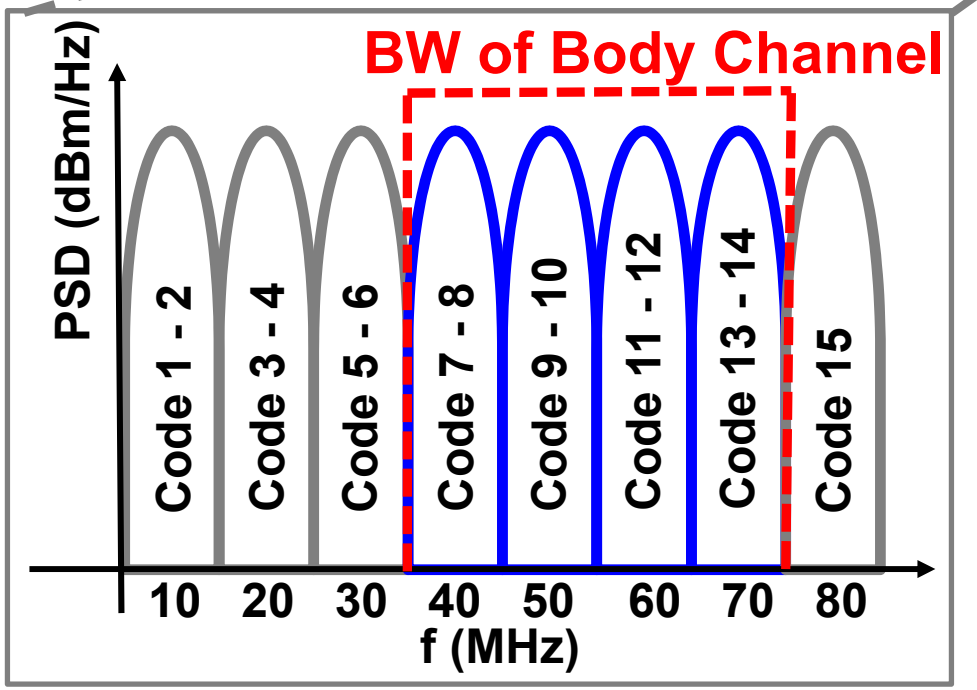
$\frac{3}{16}$ x 160Mb/s = 30Mb/s

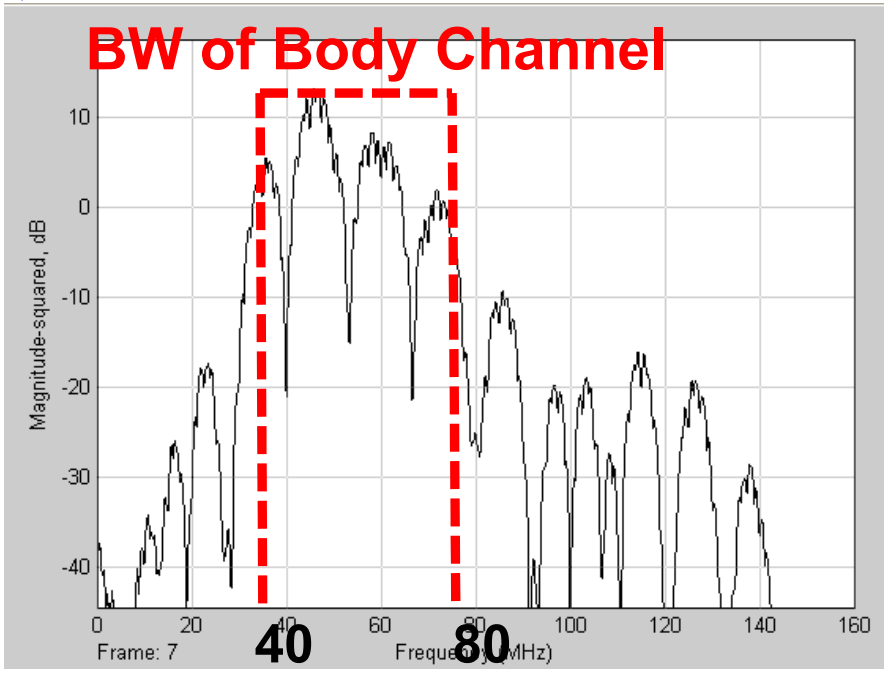
3:1 Walsh Code Modulation (Length 16)

10Ms/s

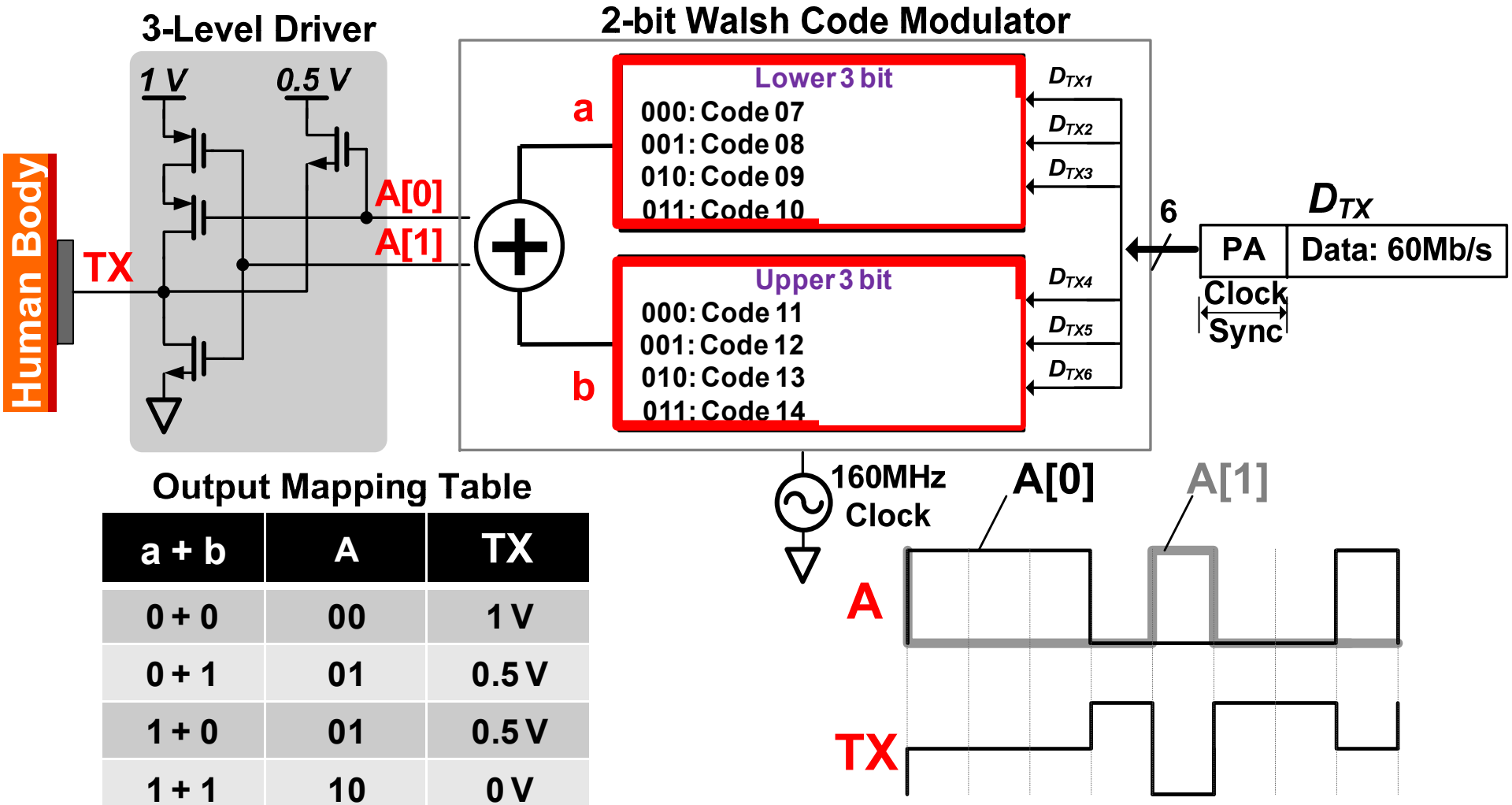
Output Data

160Mb/s





Highly Efficient Wideband TX

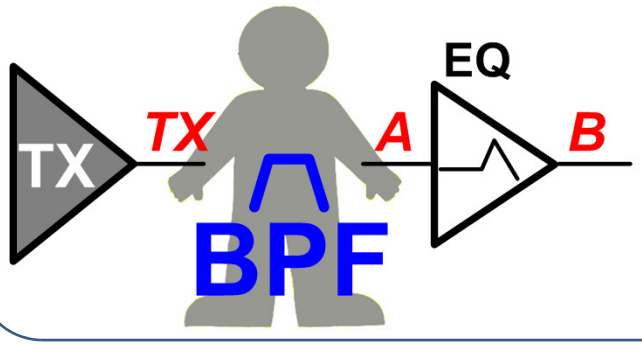


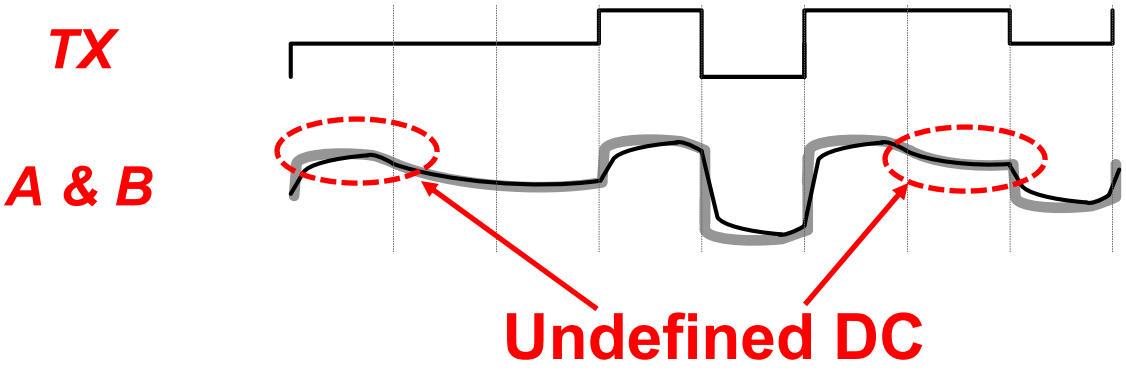
Output Mapping Table

a + b	A	TX
0 + 0	00	1 V
0 + 1	01	0.5 V
1 + 0	01	0.5 V
1 + 1	10	0 V

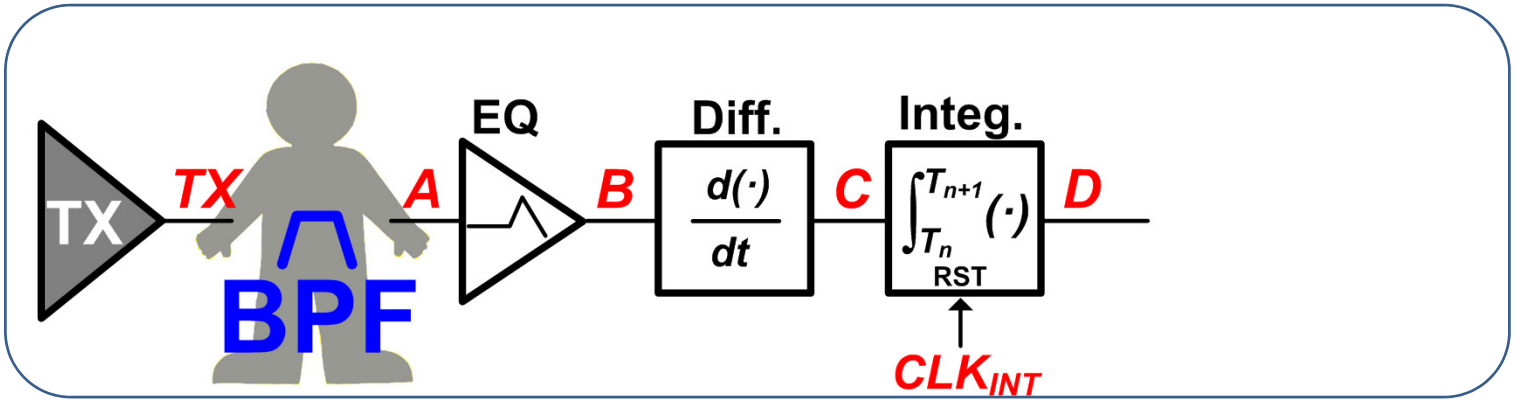
- Further enhanced data rate (60Mb/s)
- Highly efficient data transmission
- No power consuming modulation blocks

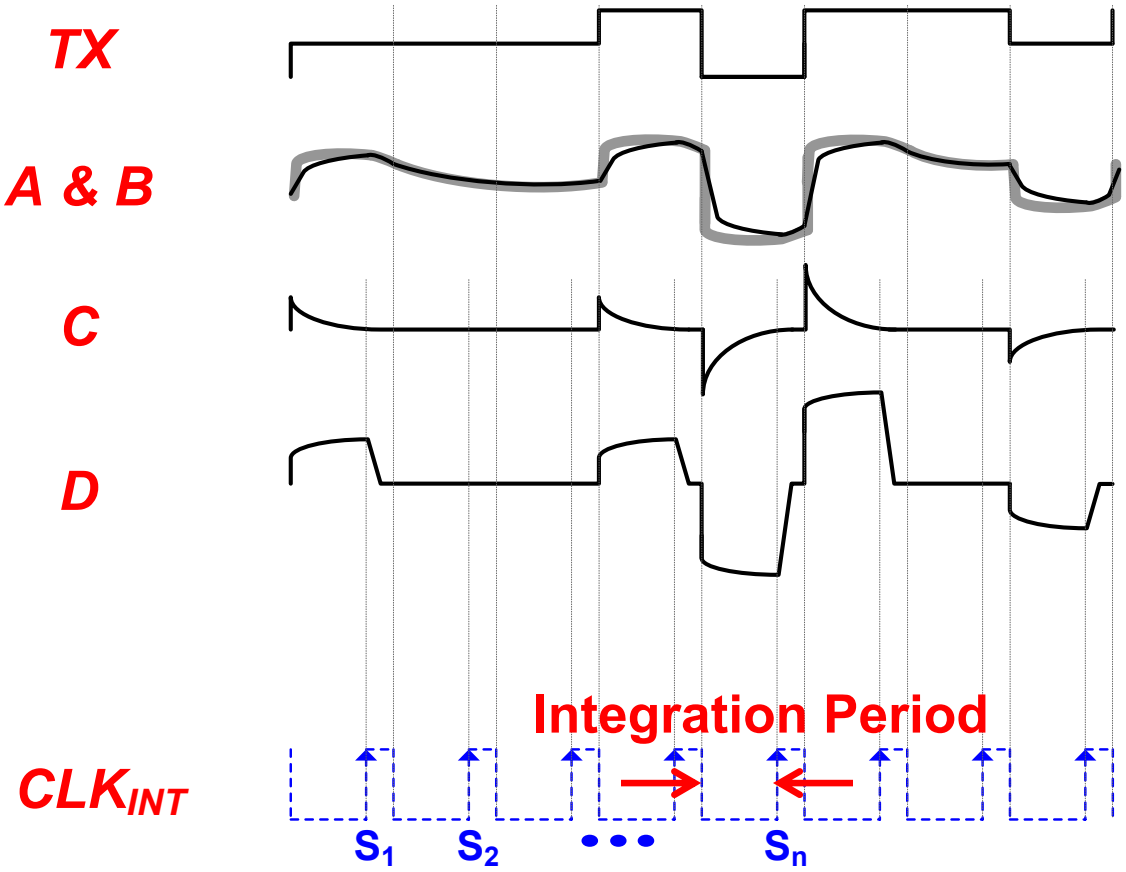
Transient Detection



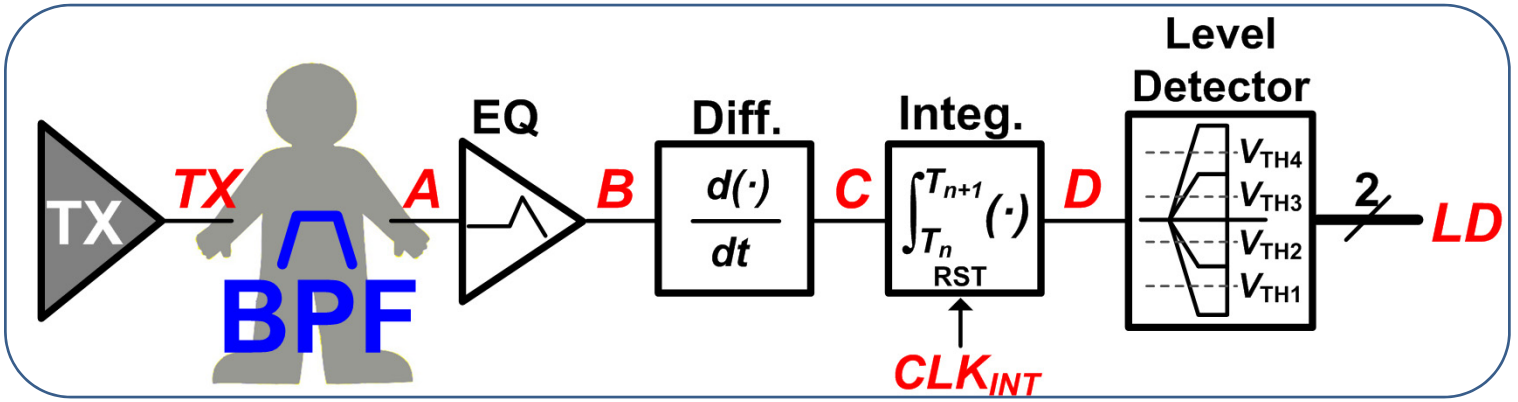


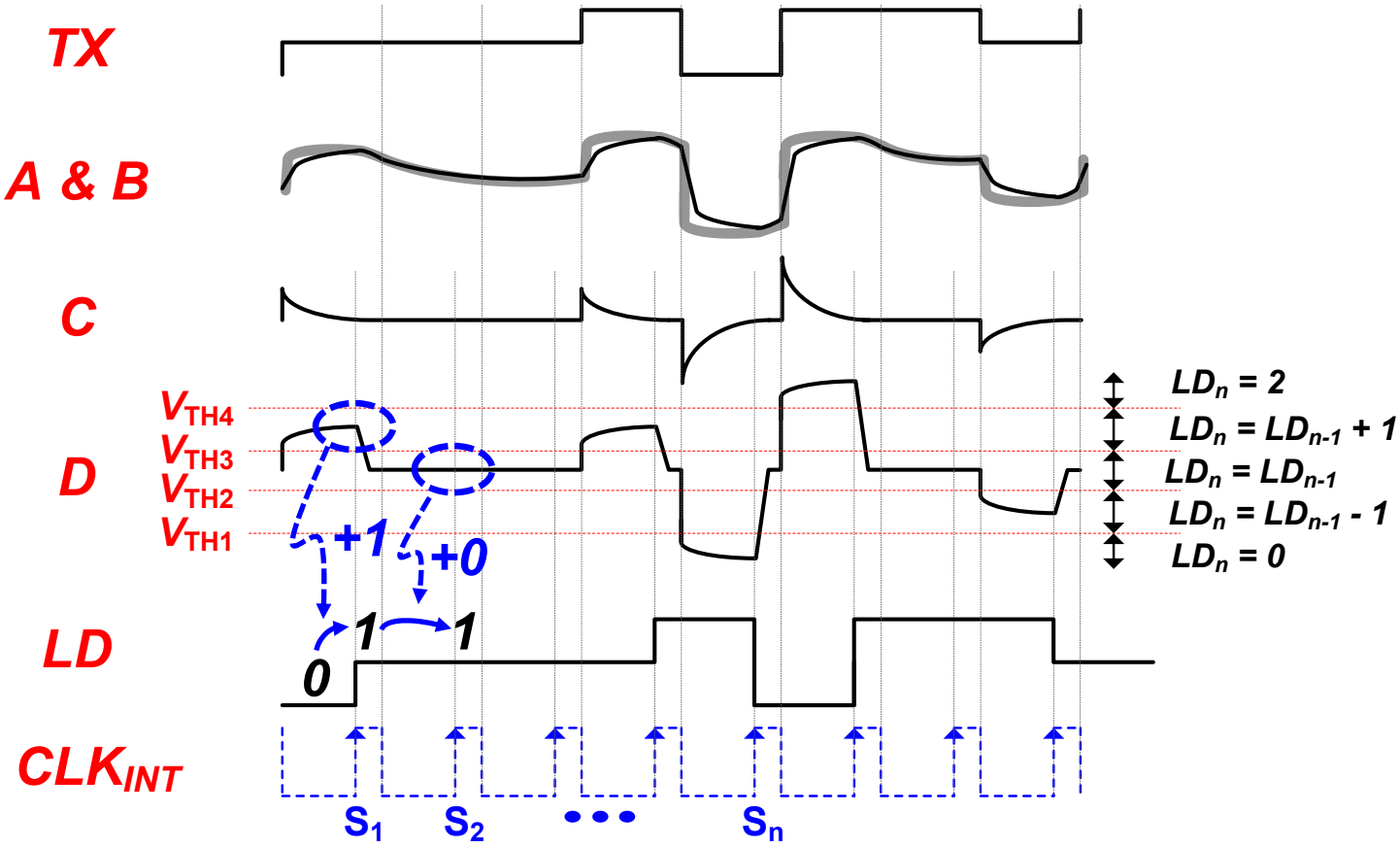
Transient Detection



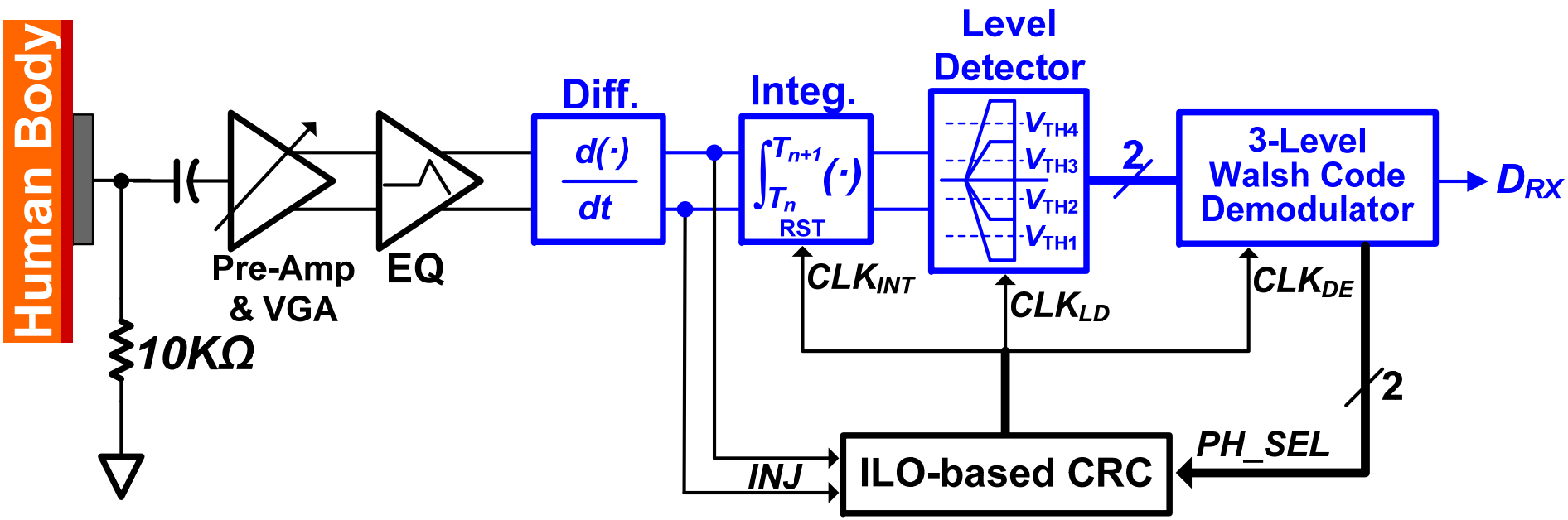


Transient Detection

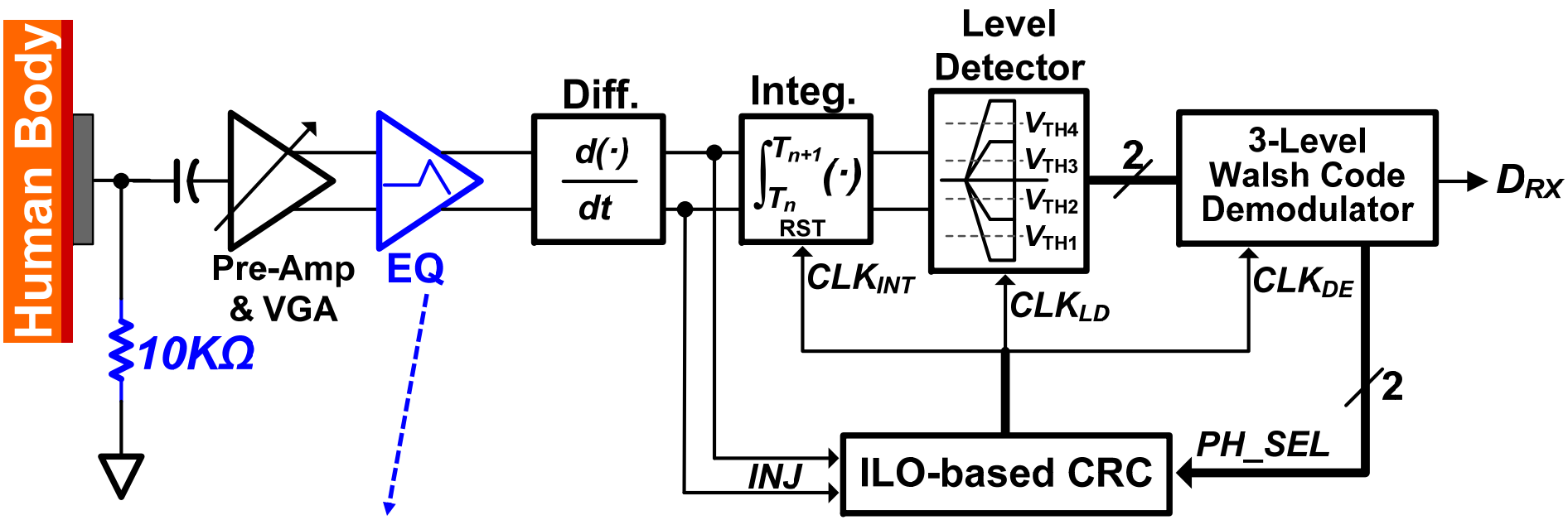


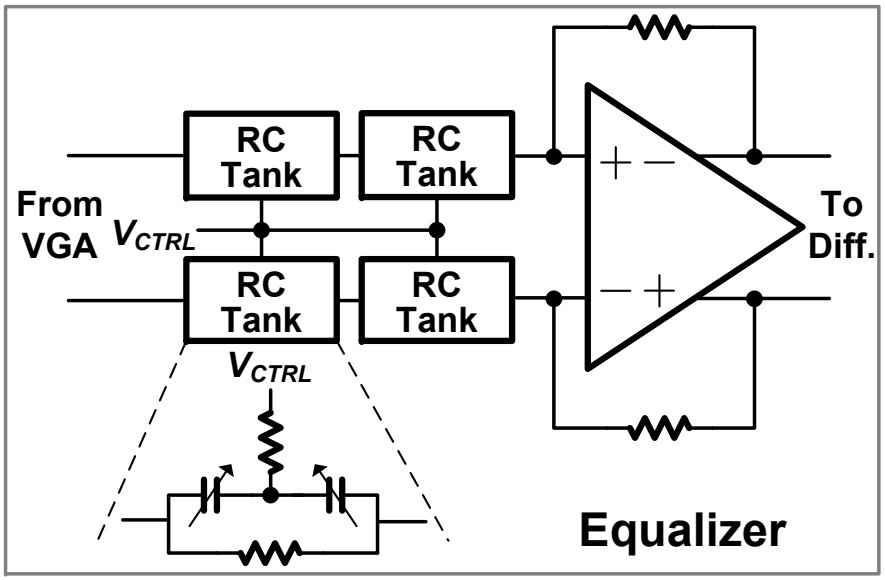


Highly Efficient Wideband RX



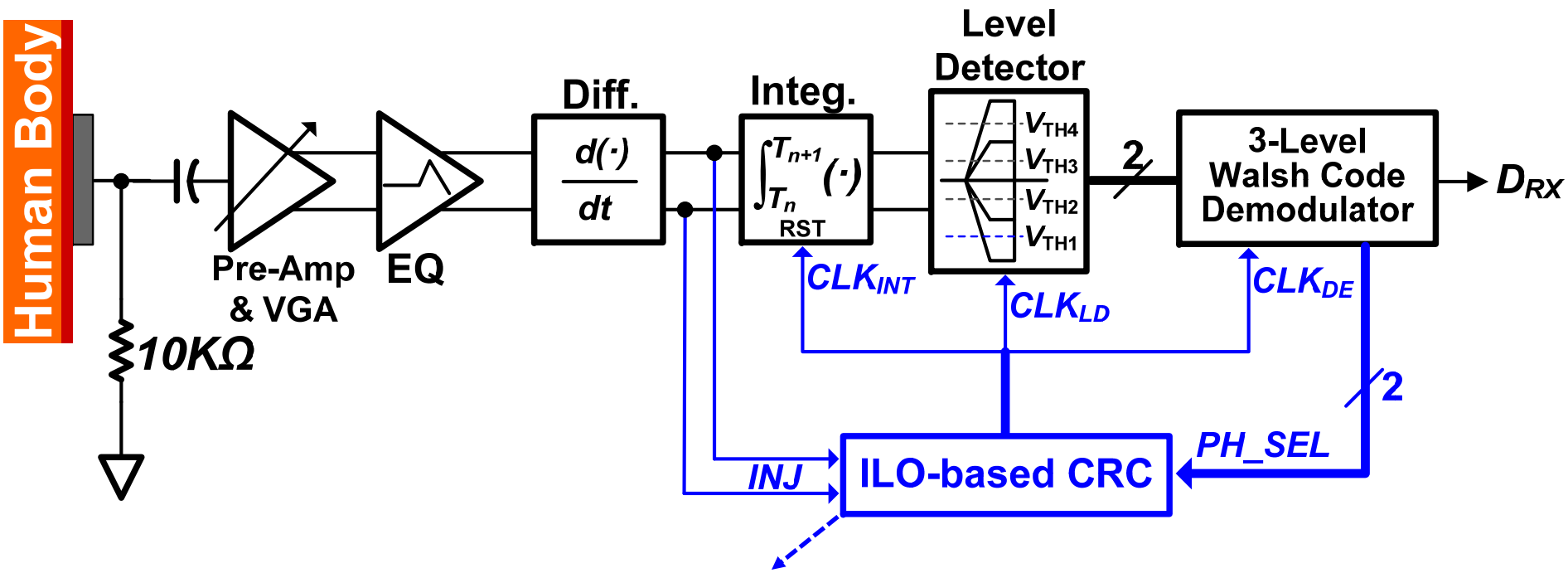
Highly Efficient Wideband RX

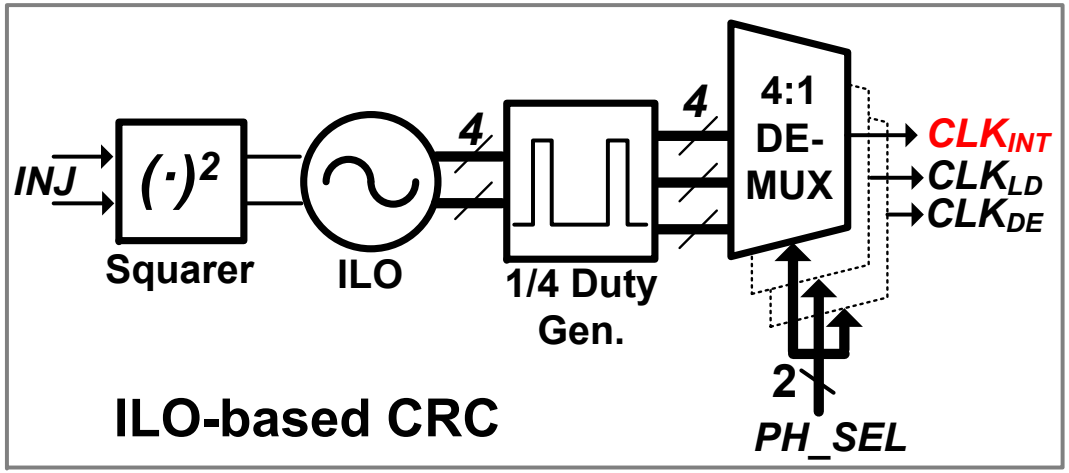




- 2nd order equalizer
- Lower channel loss
- Wider channel bandwidth

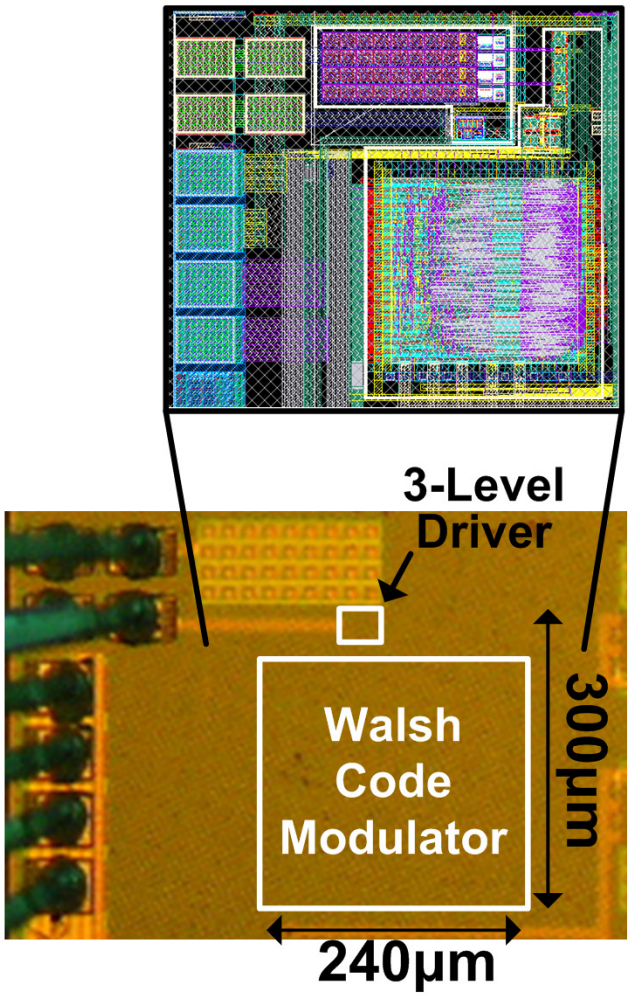
Highly Efficient Wideband RX



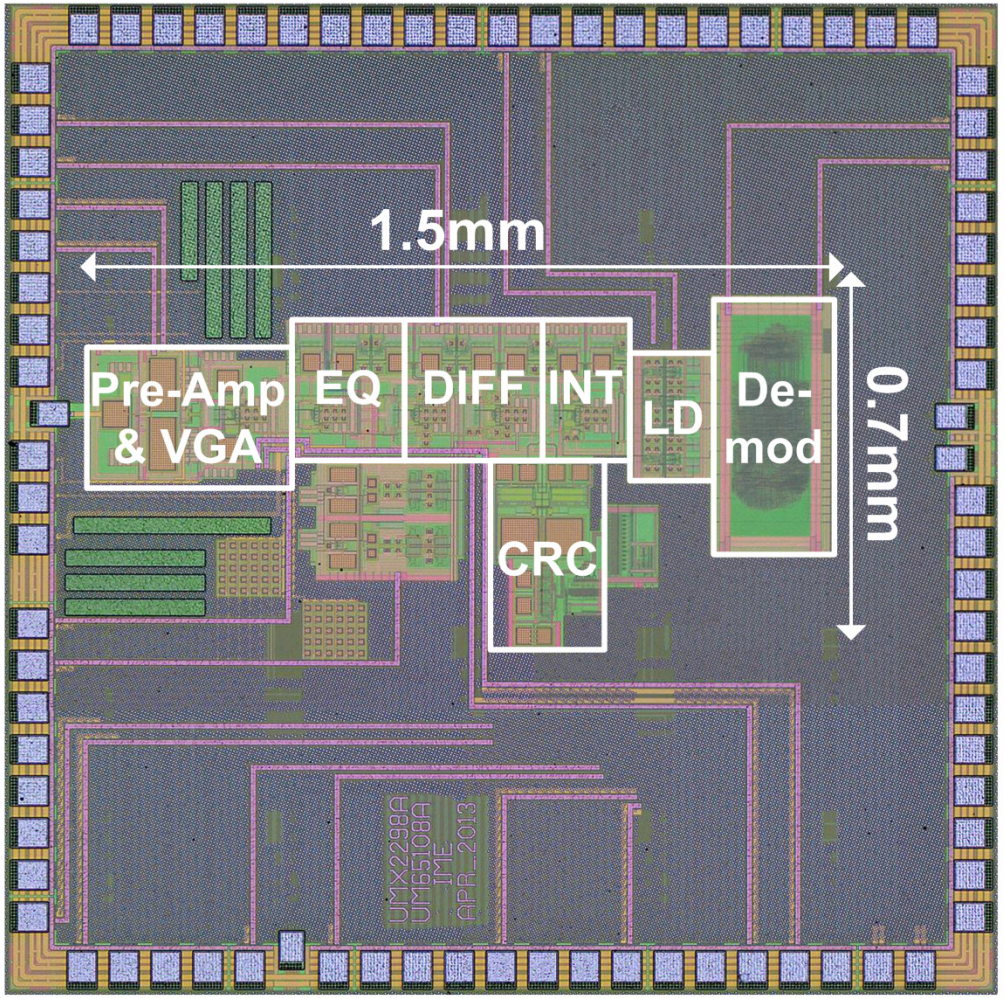


- Injection locks incoming data to recover clock
- Low power and low area
- No PLL and X-tal Osc.

Chip Micrograph



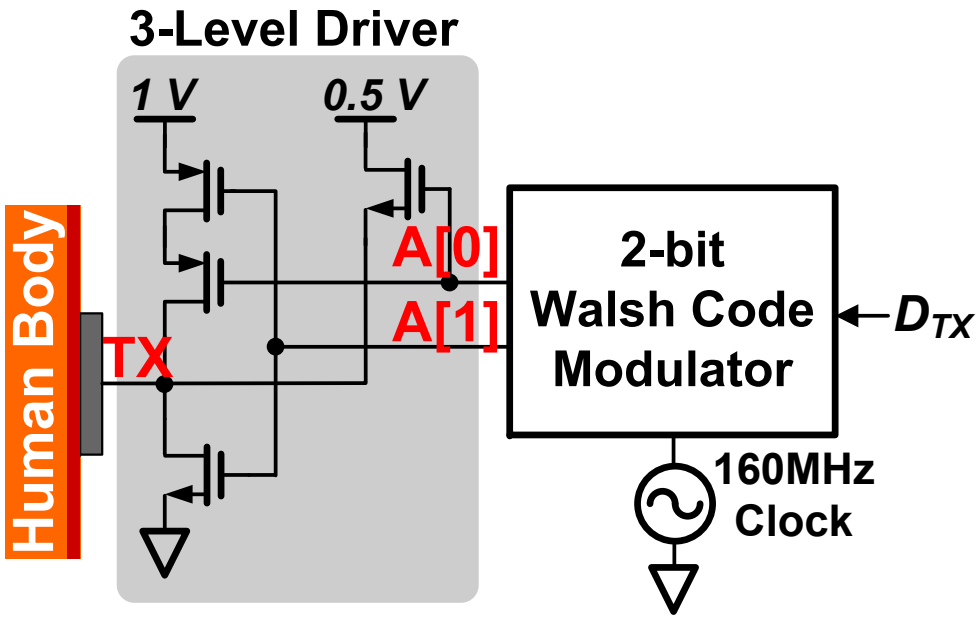
Transmitter

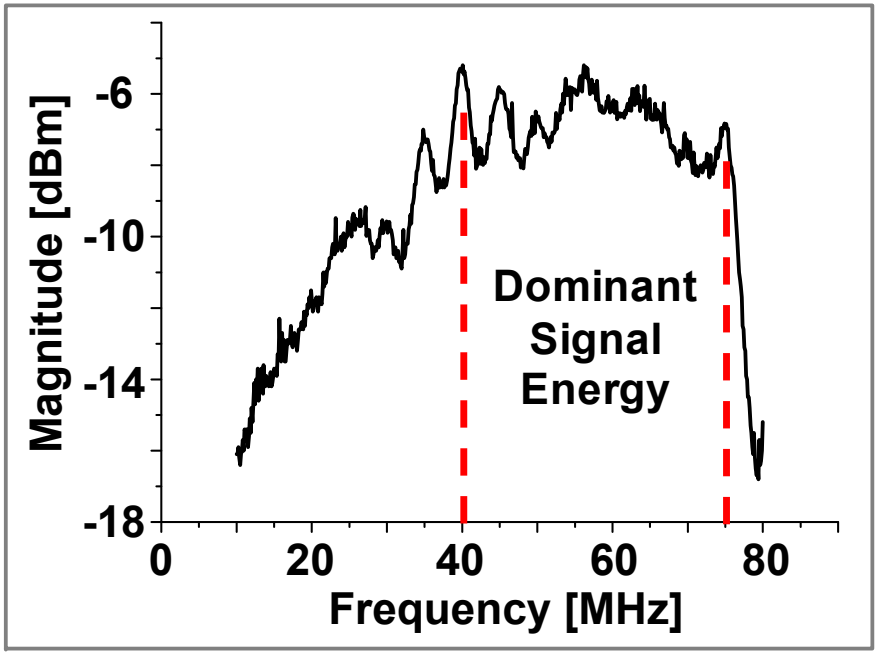


Receiver

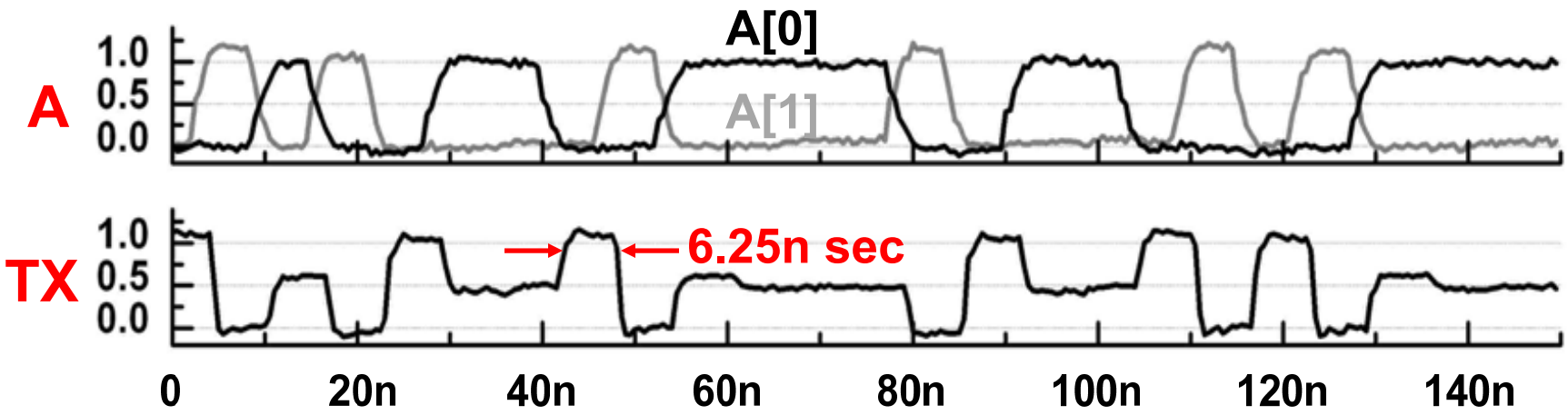
- Implemented in a 65nm CMOS process.
- Consumes 1.85mW in TX & 9mW in RX.

Measured TX Waveforms & Spectrum

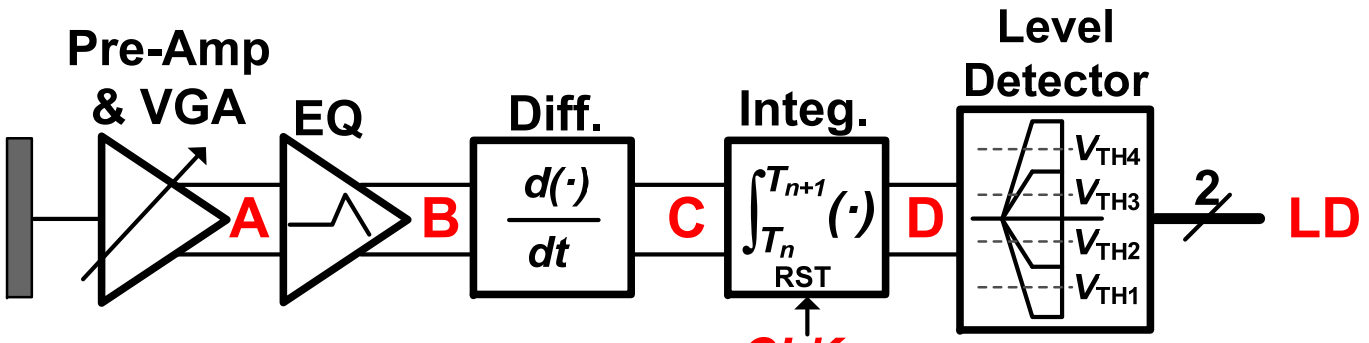


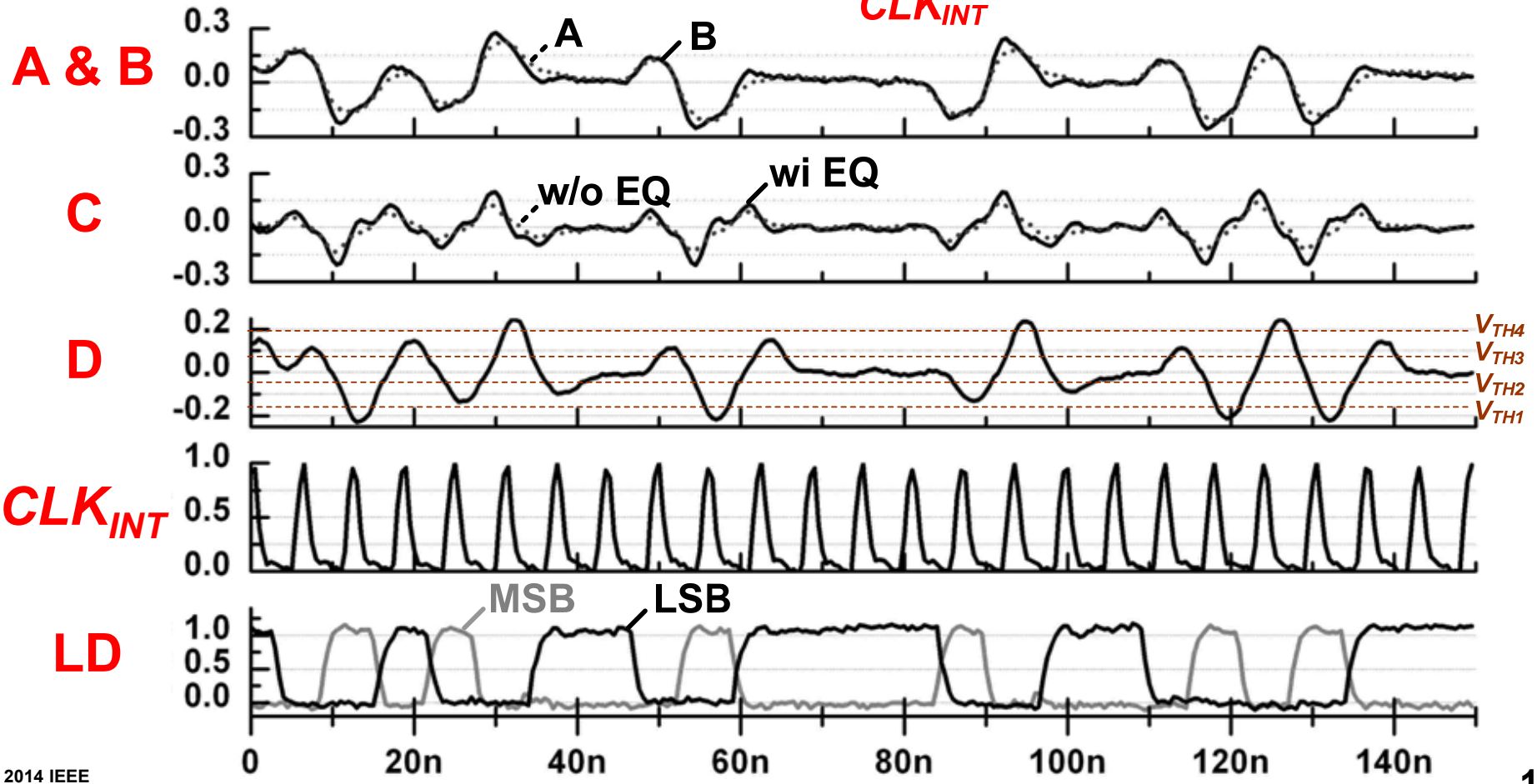


TX Output Spectrum

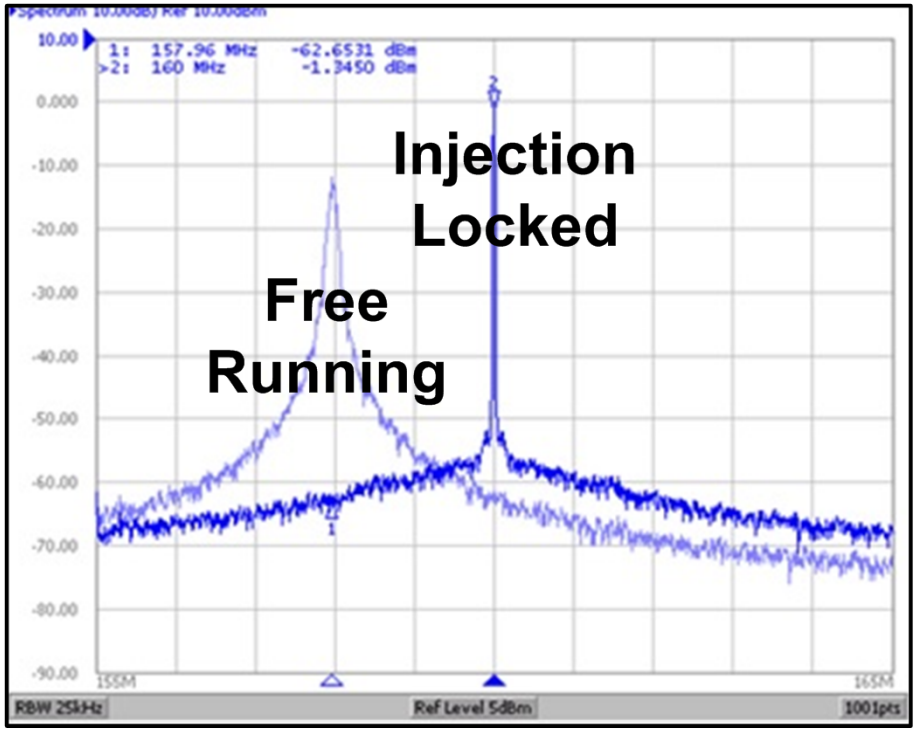


Measured RX Waveforms

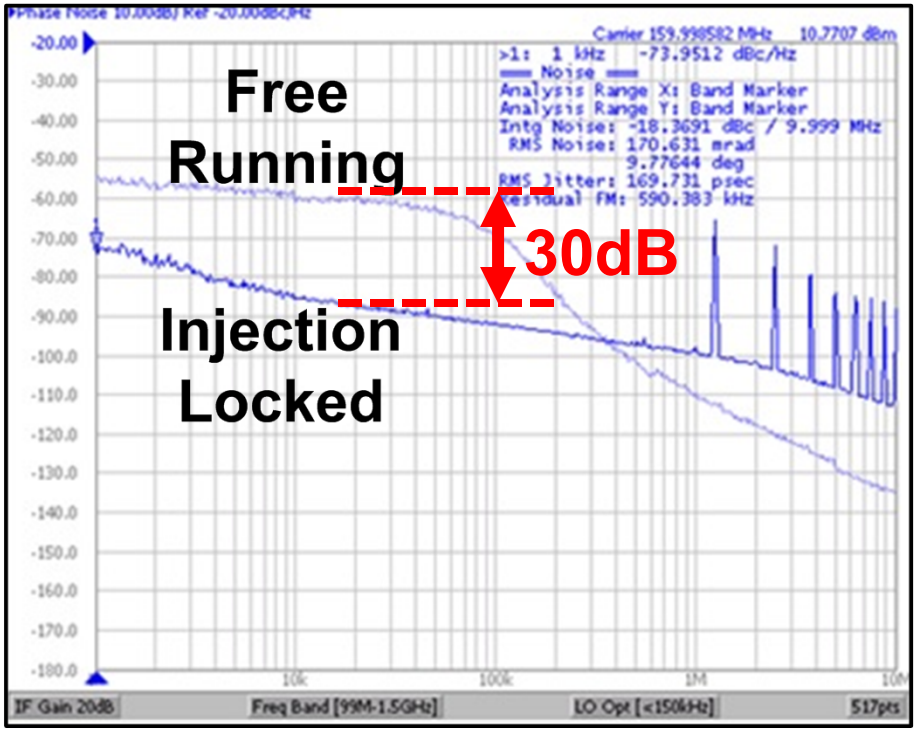




Measurement Results of ILO



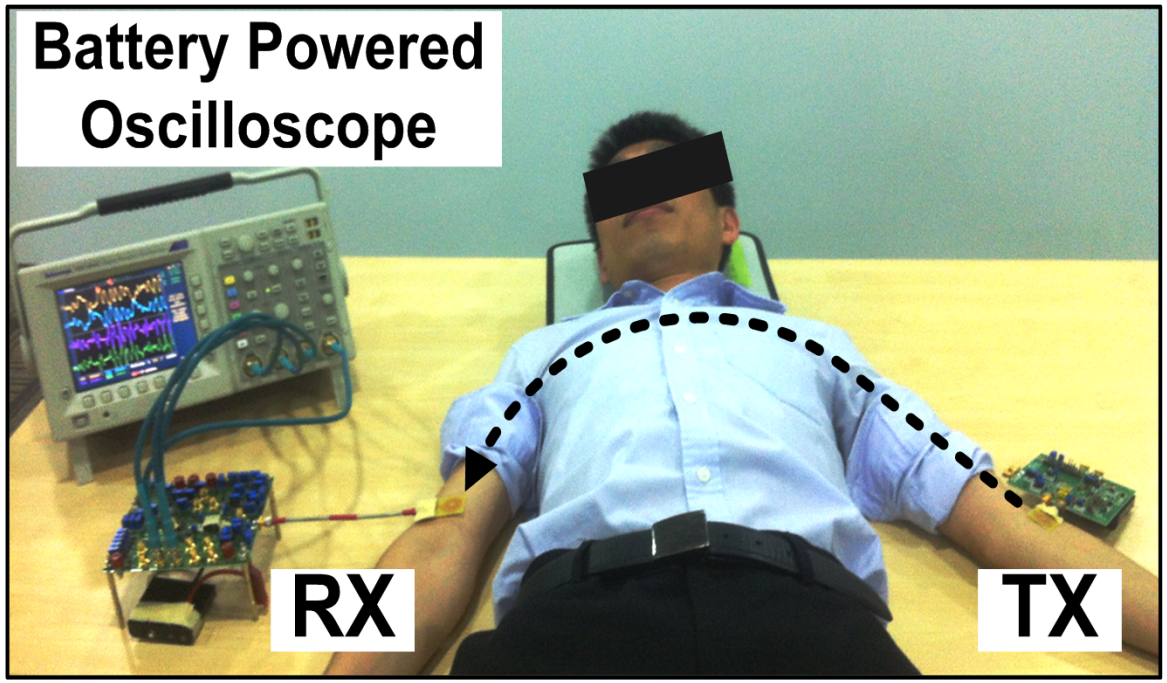
Spectrum



Phase Noise

- Recovered clock frequency: 160MHz
- RMS jitter: 170p sec

Image Data Communication Test



Test Setup

Transferred Image

- TX and RX are powered by batteries.
- Battery powered oscilloscope is used.

Performance Summary

Parameters	ISSCC '07 [1]	JSSC '09 [2]	ISSCC '09 [3]	JSSC '12 [4]	This Work
Technology [nm CMOS]	180	180	130	180	65
Supply Voltage	0.9V	1V	1.2V	1V	1.1V
Modulation	3-Level PPM	AFH FSK	Correlation Direct Digital	Double FSK	3-Level Walsh Coding
Input Impedance	50Ω	< 100Ω	Capacitive load	100–600Ω	10KΩ
Maximum Data Rate	10Mb/s	10Mb/s	8.5Mb/s	10Mb/s	60Mb/s
Sensitivity	-30dBm @ < 10^{-4} BER	-65dBm @ 10^{-5} BER	-60dBm @10^{-3} BER	-62dBm @ 10^{-5} BER	-58dBm @ < 10^{-5} BER
SIR	N.A.	-28dB @ 10^{-3} BER	N.A.	-20dB @ 10^{-3} BER	-20dB[1] @ 10^{-3} BER
Power Consumption	TX: 0.71mW RX: 1.89mW	TX: 2.4mW RX: 3.7mW	TX: 0.6mW RX: 2.15mW	TX: 2mW RX: 2.4mW	TX: 1.85mW RX: 9.02mW
Energy/bit	TX: 71pJ/b RX: 189pJ/b	TX: 240pJ/b RX: 370pJ/b	TX: 70pJ/b RX: 250pJ/b	TX: 200pJ/b RX: 240pJ/b	TX: 31pJ/b RX: 150pJ/b

[1] Robust operation mode

Summary

- **3-level direct digital Walsh-coded signaling**
  - Generates a band-limited TX output.
  - Requires no power-consuming modulation blocks.

- **High input impedance and Equalizer**
  - Achieves lower channel loss & wider channel band.

- **Transient-detection architecture**
  - Recovers the received signal which has undefined DC level with low power consumption.

- **ILO-based clock recovery**
  - Recovers the clock from the incoming data.

A 30GS/s Double-Switching Track-and-Hold Amplifier with 19dBm IIP3 in an InP BiCMOS Technology

Timothy Gathman[1,2], Kristian Madsen[1,3]
James Li[4], Thomas Oh[4], James Buckwalter[1]

[1]University of California San Diego, La Jolla, CA
[2]Qualcomm Technologies, Inc., San Diego, CA
[3]Anokiwave, San Diego, CA
[4]HRL Laboratories, Malibu, CA

Outline

- High-Speed / High-Linearity Sampling
  - Applications
  - Motivations
- An InP BiCMOS Technology
- Double-Switching THA Architecture
- Measurement Results

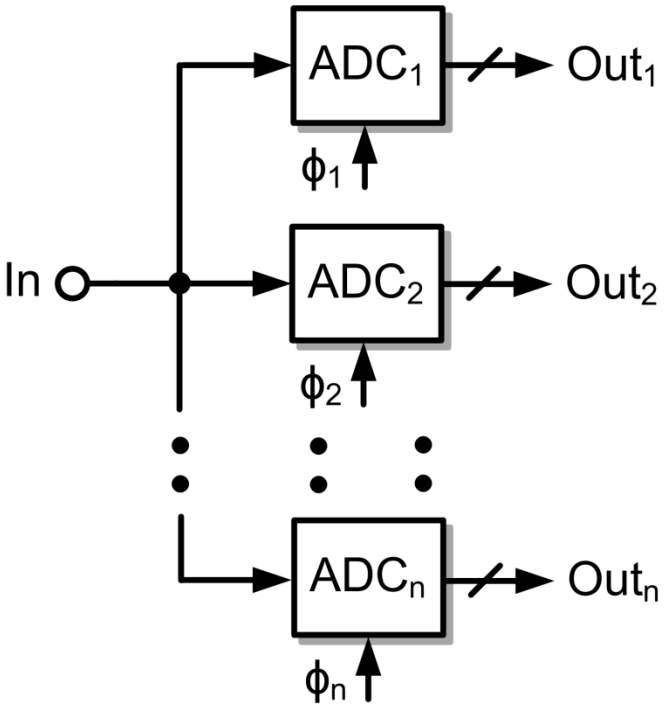
High-Speed/High-Linearity Sampling

Demand for high-speed ADCs driven by:

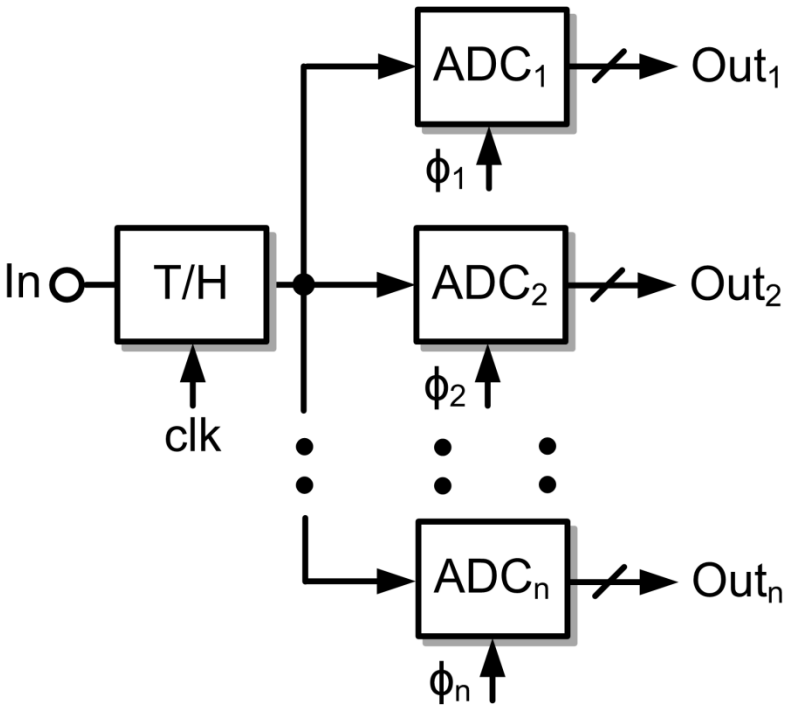
→ Short and long range optical communication standards

→ High resolution T/M → Wideband RF sampling

Time Interleaved ADC Architecture

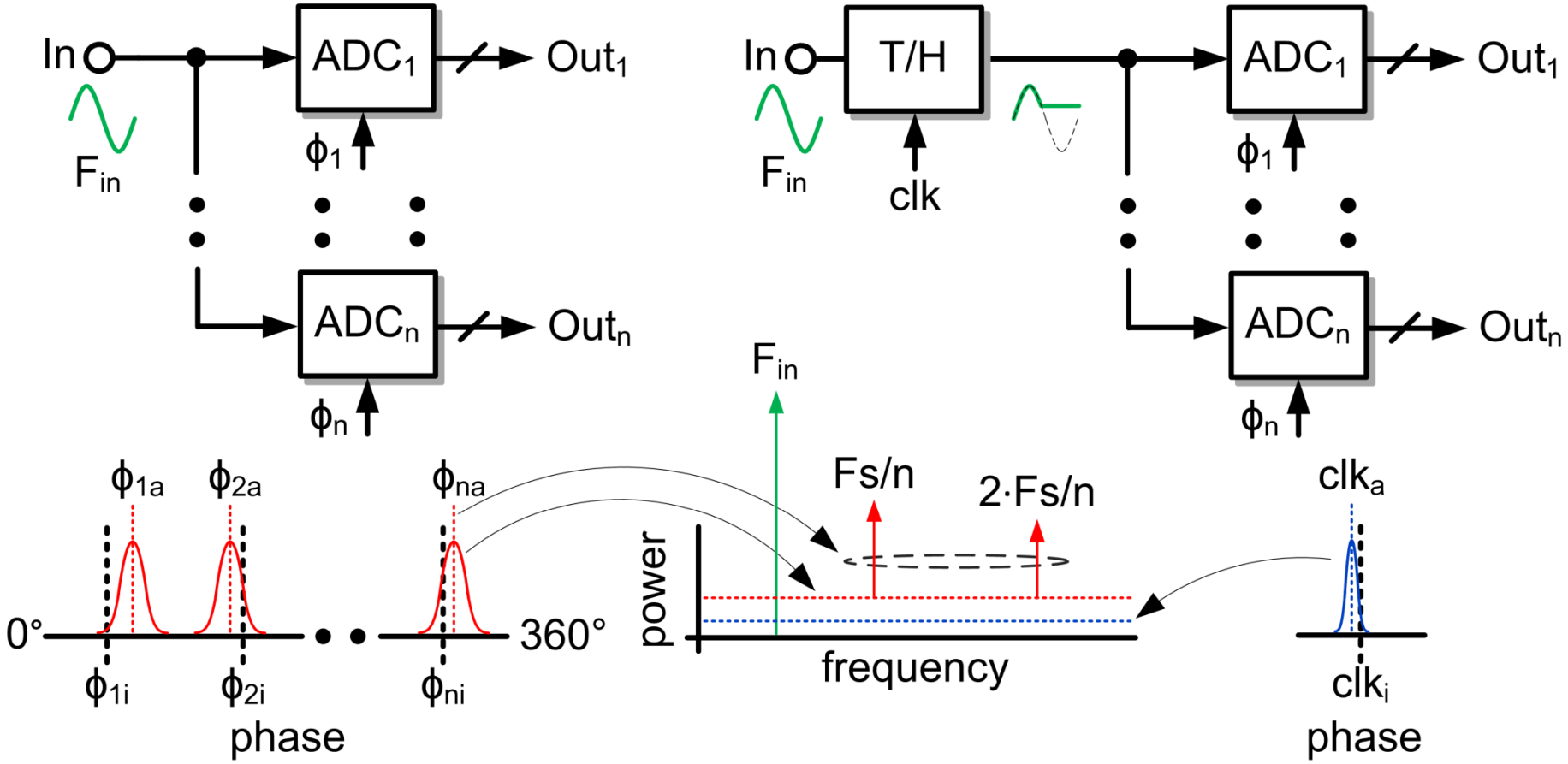


T/H-First Time Interleaved ADC



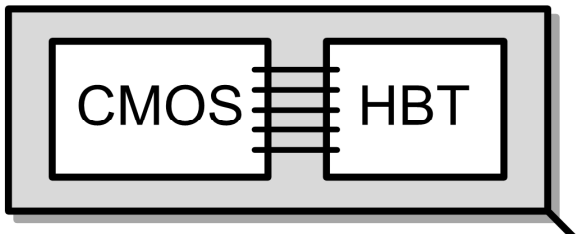
S. Verma, et. al, E. Janssen, et. al, B. Setterberg, et. al, and H.K. Hong et. al. ISSCC '13

High-Speed/High-Linearity Sampling



- T/H alleviates spurs generated by phase skew between ADCs
- Enables constant distortion across frequency
- Goal: >30GS/s with >8-bit linearity – requires HBT T/H

Integration of CMOS & HBT



Multiple Substrates Packaged With Interconnects

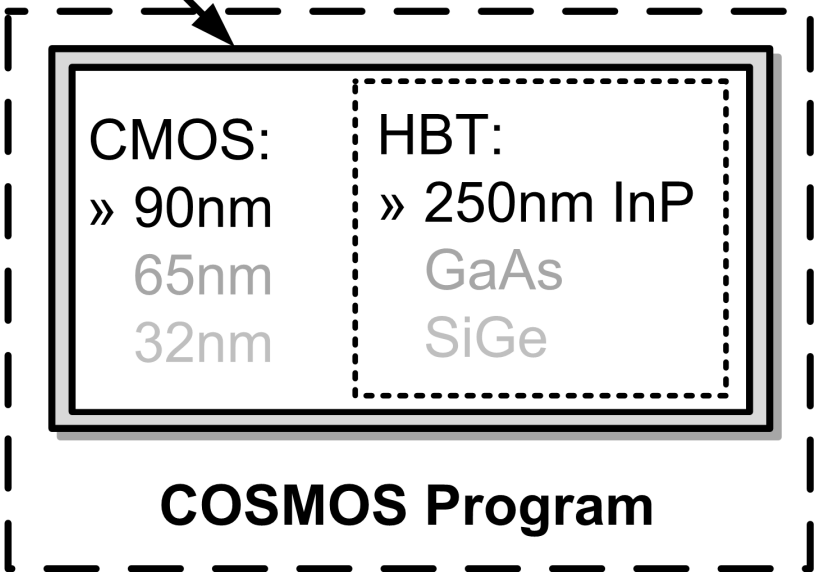
- Many Integration Choices
- Degraded Signal Integrity
- Limited Number of Interconnects

Single Substrate

- Intimate Integration
- Slower Technological Development

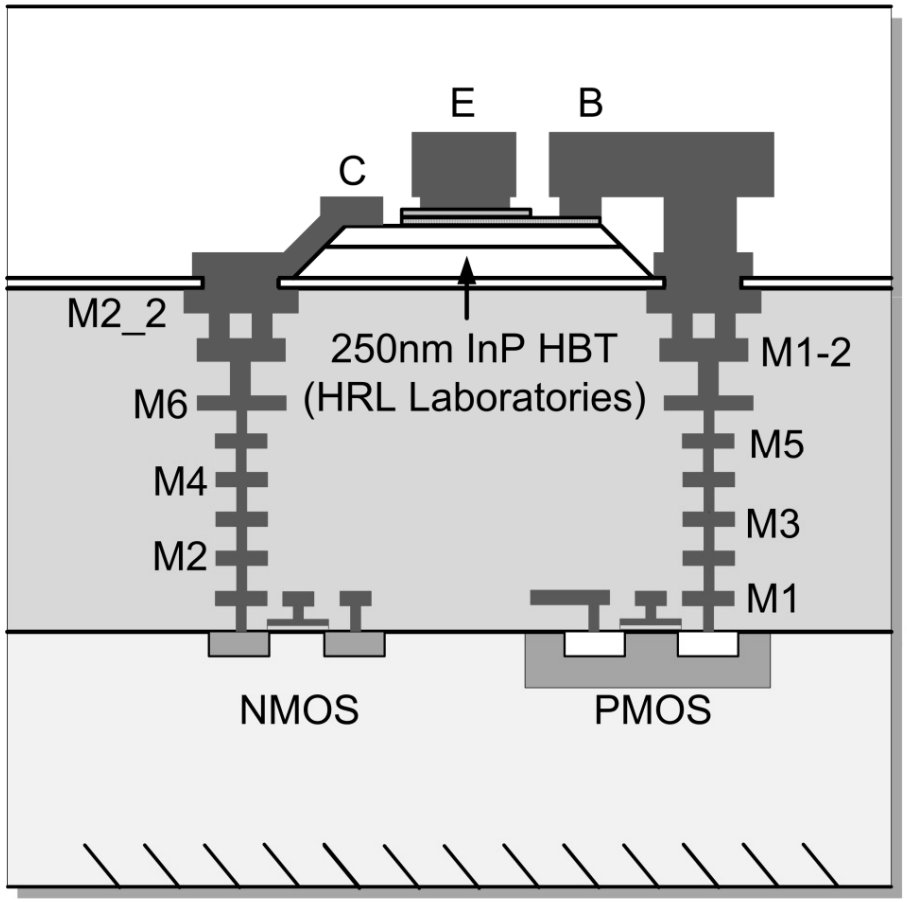
Heterogeneous Integration

- Co-existence of High Performance Bipolar Devices & Scaled CMOS
- Minimizes Interconnect Losses



J. C. Li. et al. "Circuit Applications of Hererogeneously Integrated InP HBTs on RF-CMOS." Communications, Microelectronics, Optoelectronics, and Sensors Emerging Technologies Symposium. July 2013.

InP BiCMOS Integration

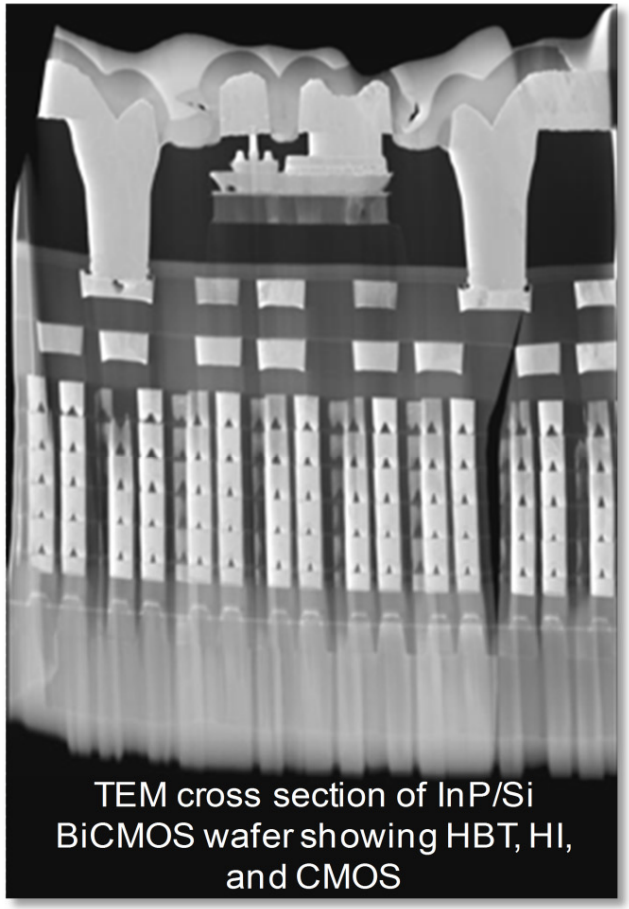


InP HBT + Interconnect

Adhesive

IBM BEOL

IBM 90nm CMOS

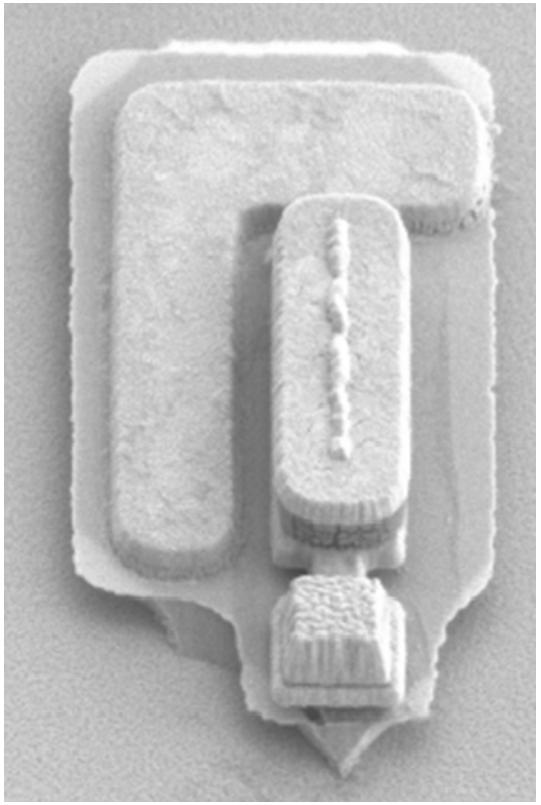


- InP epitaxial wafer is bonded to top layer of CMOS wafer via an adhesion layer. The DHBTs are then processed and interconnects are added to connect to the underlying CMOS.

J. C. Li. et al. "Circuit Applications of Hererogeneously Integrated InP HBTs on RF-CMOS." Communications, Microelectronics, Optoelectronics, and Sensors Emerging Technologies Symposium. July 2013.

The HRL COSMOS G4 Process

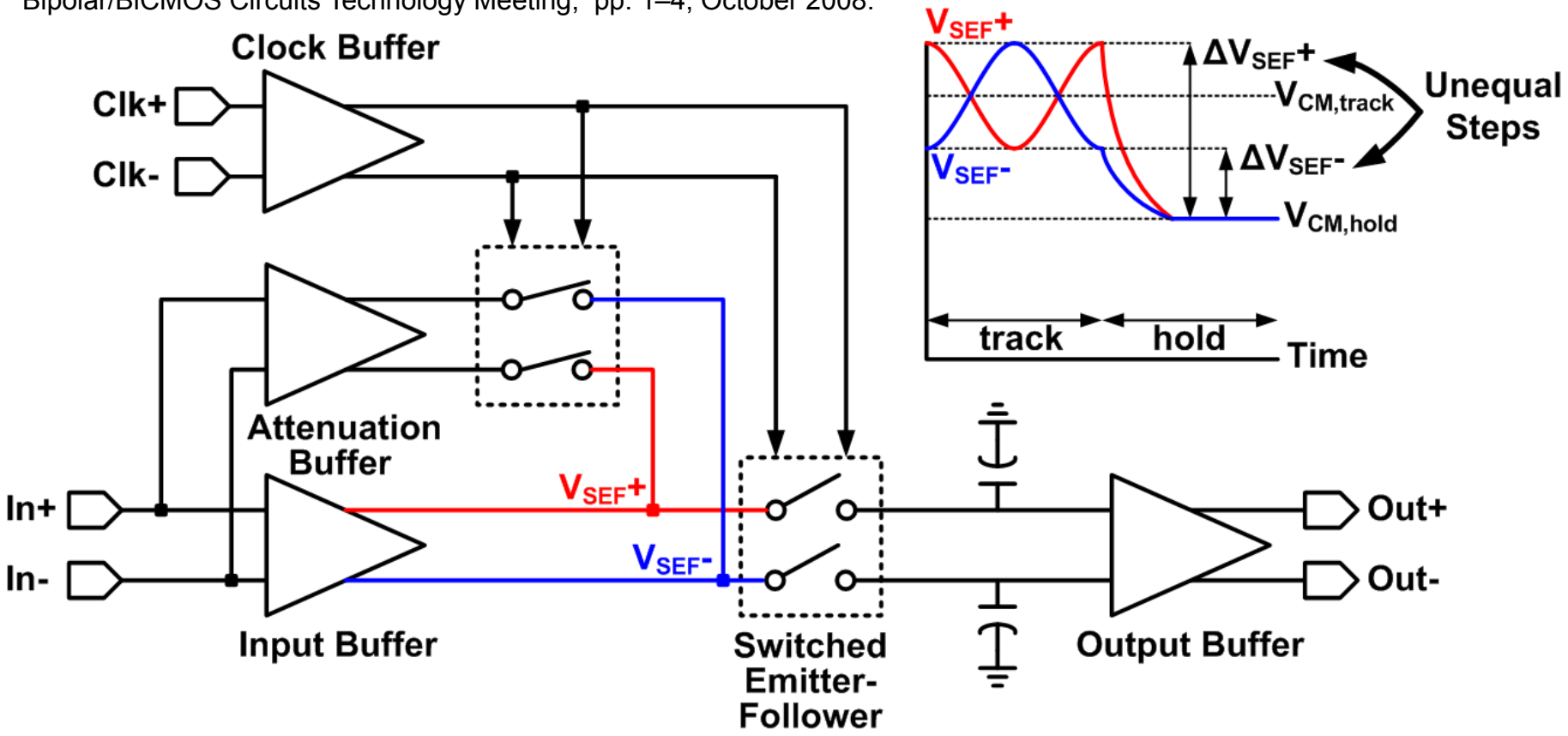
- 250 nm wide emitter InP HBT
  - 300GHz f_t/f_{max} is attainable in this process
  - 2 metal interconnects
- IBM 90nm CMS9FLP
  - Vdd = 1.2/2.5V
  - 8 BEOL Metals
  - 140 GHz f_t/f_{max}
  - Backend passives, MIM, VN Cap, KXRES
- ~10μm interconnect distance between CMOS and InP HBT



J. C. Li, et. al. "Leveraging Heterogeneous Integration with Deep Sub-Micron InP DHBTs." Communications Microsystems Optoelectronics Sensors Emerging Technologies Workshop, 2010.

State-of-the-Art THA Architecture

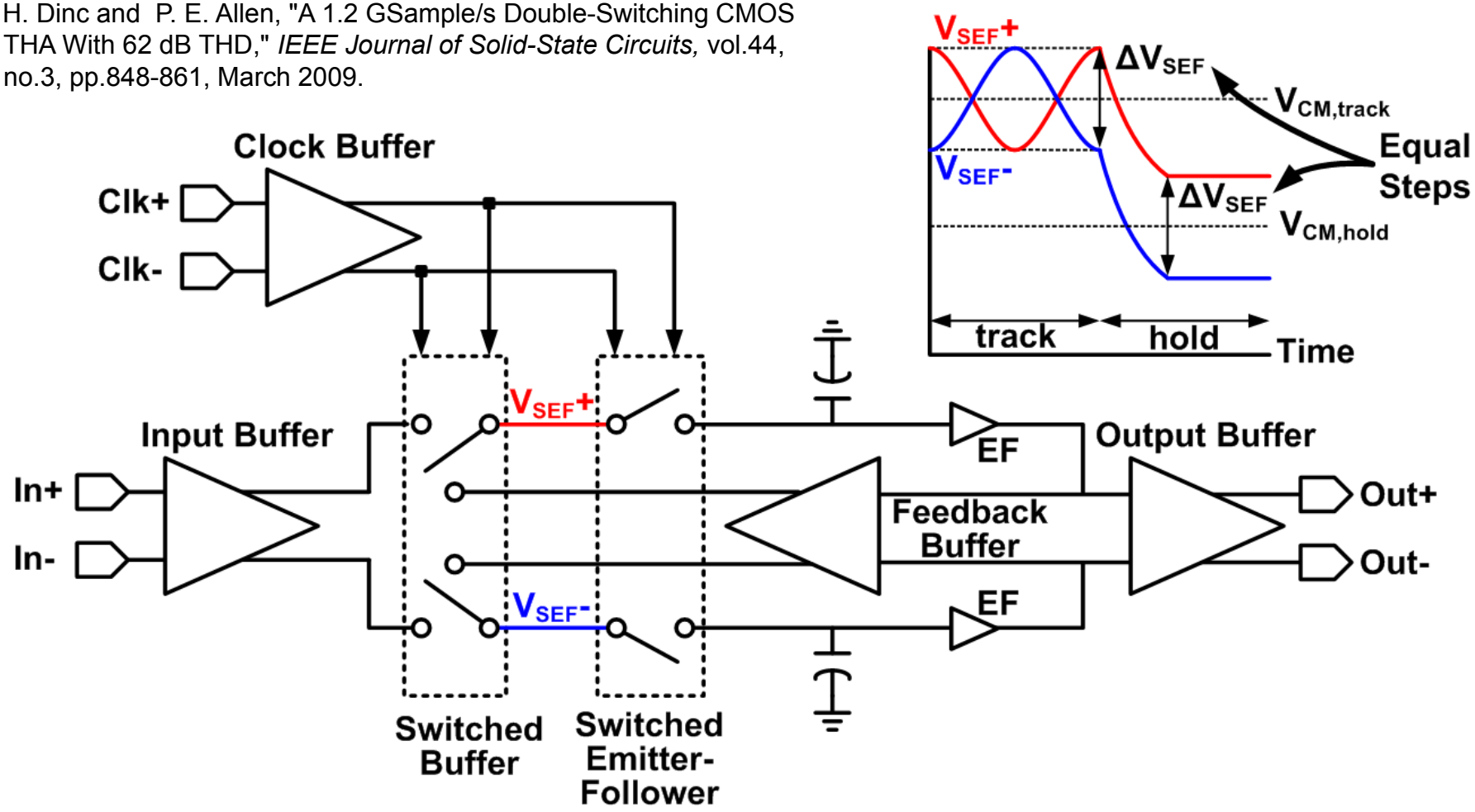
X. Li *et al*., "A 40 GS/s SiGe track-and-hold amplifier," IEEE Bipolar/BiCMOS Circuits Technology Meeting, pp. 1–4, October 2008.



- Feedthrough attenuation buffer improves isolation
- Unequal voltage steps during sampling process creates nonlinear pedestal error on sampled voltage

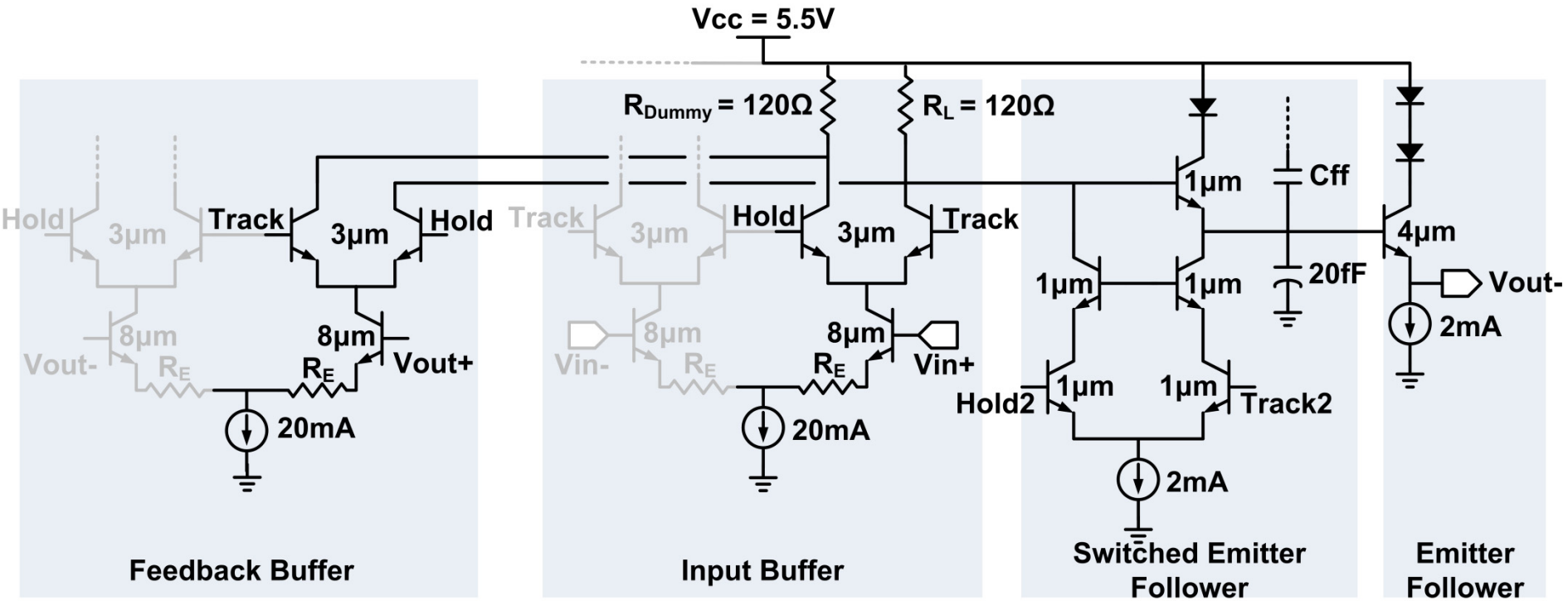
Double-Switching THA Architecture

H. Dinc and P. E. Allen, "A 1.2 GSample/s Double-Switching CMOS THA With 62 dB THD," *IEEE Journal of Solid-State Circuits,* vol.44, no.3, pp.848-861, March 2009.



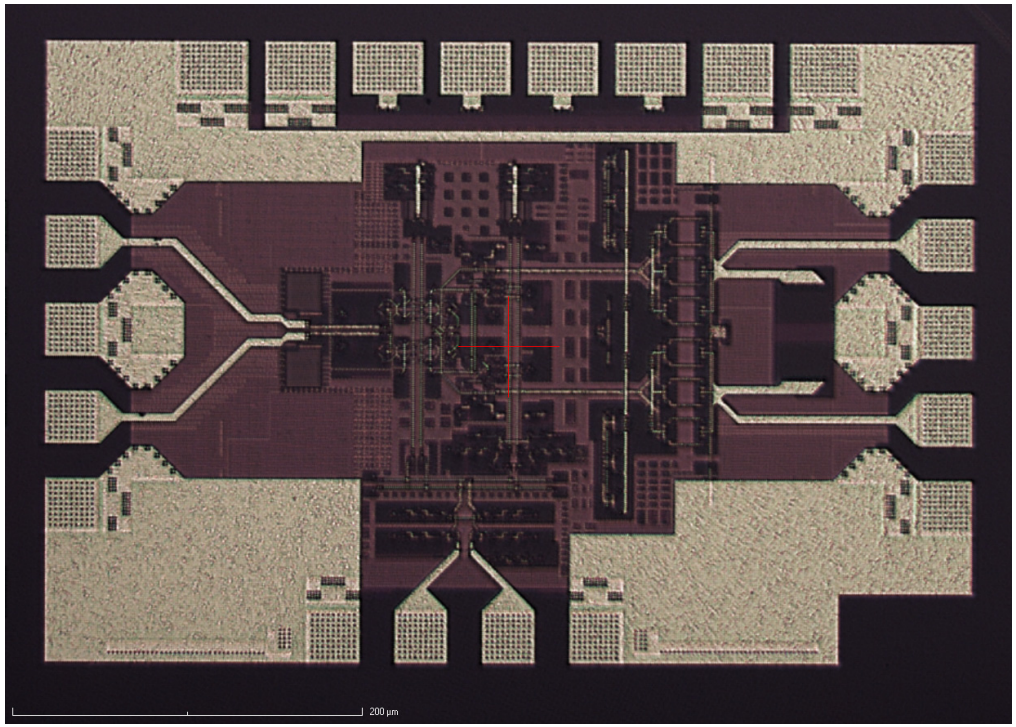
- Reduces nonlinear pedestal error and improves linearity
- Excellent linearity at high sampling rates

Double-Switching THA



- Input buffer tracks the input waveform on the SEF
- Switched Emitter Follower (SEF) samples signal on to hold capacitor of 20 fF
- Double switching buffers improve linearity and isolation

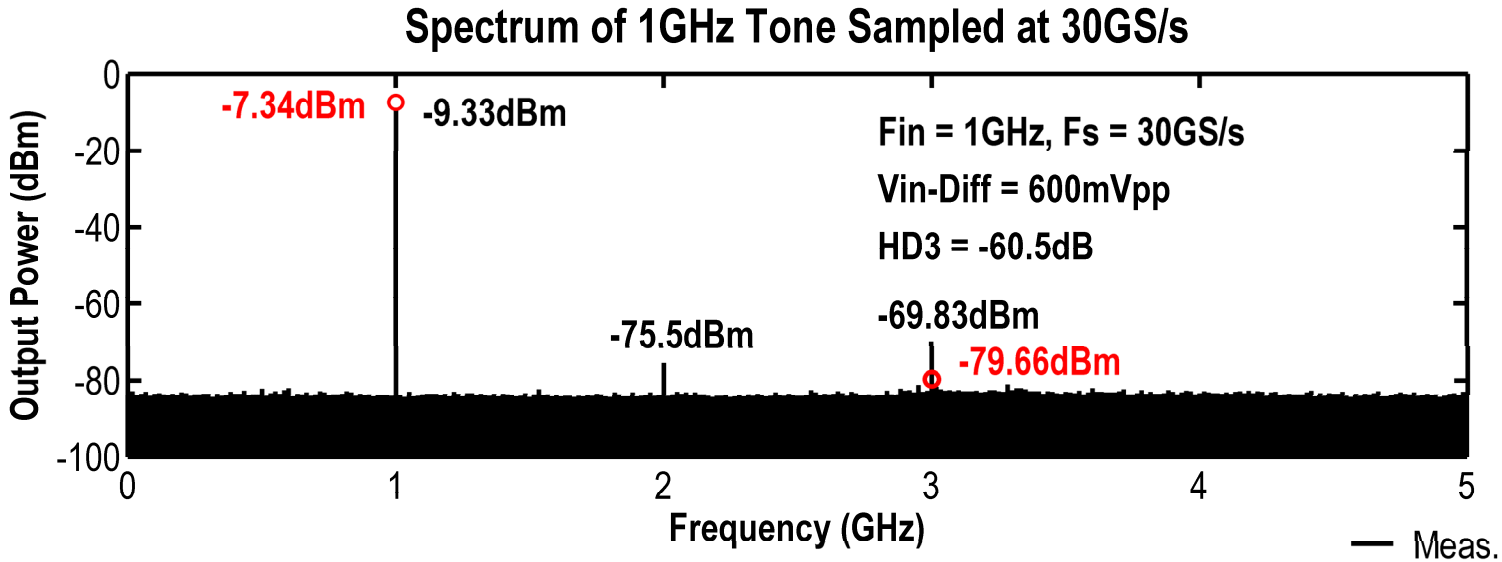
Measurement Results

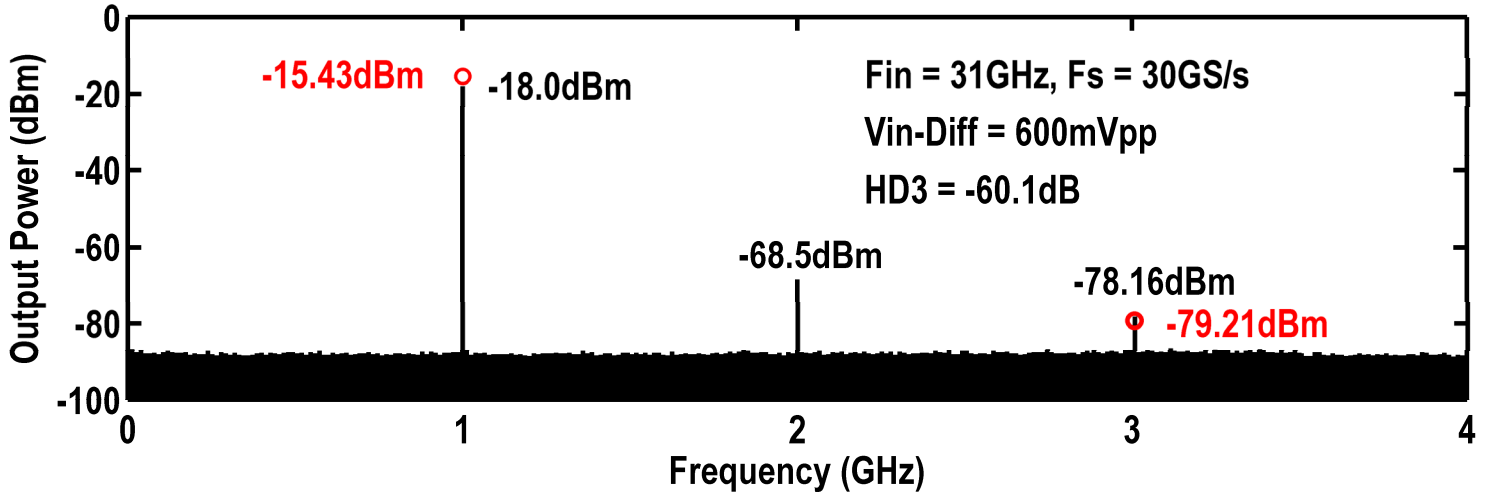


Stage	Power
T/H	266mW
Clock Driver	154mW
Output Buffer	350mW
Total Power	770mW
Total Power*	420mW
*Excluding Output Buffer	

- Fabricated in HRL COSMOS technology using > 140 InP DHBTs on IBM CMOS 9SF. Utilizes metal interconnects and back-end passives from CMOS process.
- Area: 1.1mm x 0.7mm
- Supply 5.5V

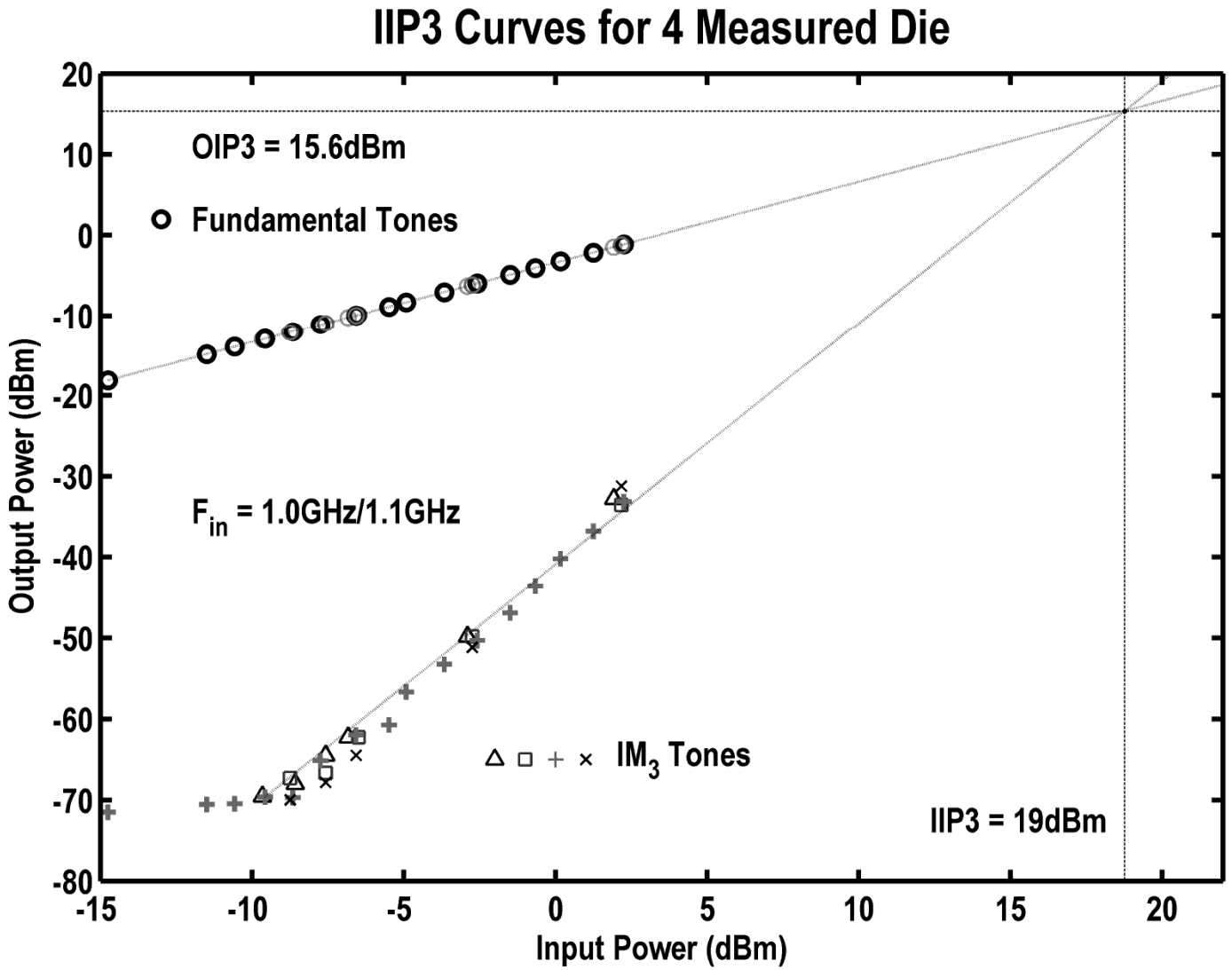
Measurement Results





- >9bit linear at 30GS/s

Measurement Results



- Consistent linearity measurement

Comparison To Previous Work

Reference	Li et. al. BCTM '08	Dinc et. al. JSSC '09	Yamanaka et. al. TMTT '10	Deneshgar et. al. CSICS '12	This Work
Process / fT	SiGe / 200 GHz	CMOS 180nm	InP / 175 GHz	InP / 400 GHz	InP / 300 GHz
Architecture	Feedthrough Attenuation	Double Switching	Feedthrough Attenuation	Uncompensated	Double Switching
Supply	5.5V	1.8V, 3.3V	-5.2V	-2.5V, -5.0V	5.5V
Fsample	40GS/s	1.6GS/s	20GS/s	50GS/s	30GS/s
Input Amplitude	1.0Vpp	400mVpp	500mVpp	-	600mVpp
THD Fin	-32.4dB 10GHz	-60dB ≤ 0.8GHz	-45dB 0.9GHz	-	< -59dB 1GHz
IIP3 / OIP3 Fin	-	-	-	17.2dBm/6.2dBm 18GHz	19dBm/15.6dBm 1GHz
Power Consumption	560mW	258mW*	735mW	1025mW*	420mW*
Area	1.8x1.0mm^2	1.47x1.36mm^2	2.0x2.0mm^2	0.675x1.075mm^2	1.1x0.7mm^2

*Excludes power consumption of the output buffer.

- Exceeds the linearity of published >20GS/s THAs using the Feedthrough Attenuation architecture
- Comparable linearity with CMOS implementation >18X increase in speed

Conclusion

- Co-integration of InP HBT and CMOS process
- 18x increase in sampling rate of double switching track-and-hold implemented in CMOS
- >9 bit linear at 30GS/s
- Highest linearity of BiCMOS track-and-holds in 20-40GS/s regime

Acknowledgements

DARPA / AFRL for their sponsorship of this work under the COSMOS program as a subcontract from HRL Laboratories, Malibu, CA.

Additional thanks goes to Daniel Zehnder at HRL for measurement assistance.

Thank you to the HSIC group at UCSD for their helpful discussion.

Normally-Off Computing with Crystalline InGaZnO-based FPGA

T. Aoki, Y. Okamoto, T. Nakagawa,
M. Ikeda, M. Kozuma, T. Osada, Y. Kurokawa,
T. Ikeda, N. Yamade, Y. Okazaki, H. Miyairi,
M. Fujita*, J. Koyama, S. Yamazaki

Semiconductor Energy Laboratory, Atsugi, Japan
**University of Tokyo, Tokyo, Japan*

Outline

- Background / Motivation
- Fine-Grained Normally-Off Computing
- Nonvolatile Register
- Prototype Chip
- Summary

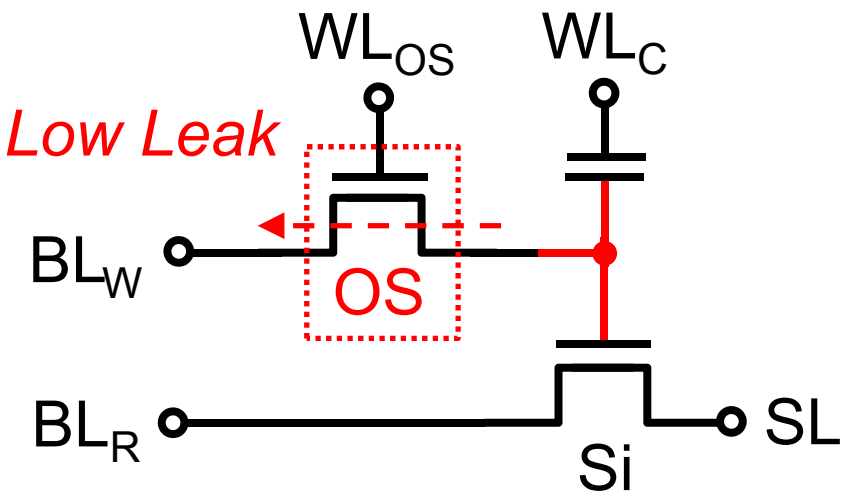
Background (1/2)

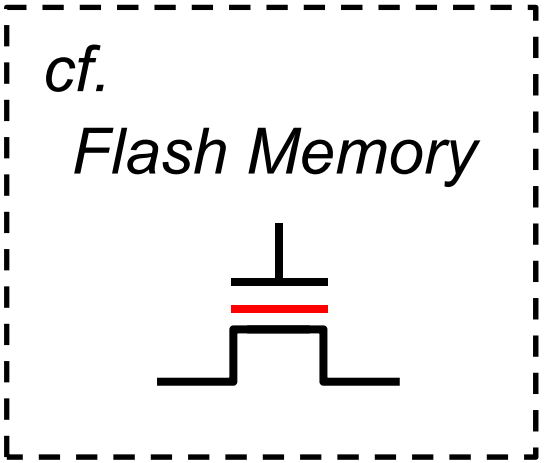
CAAC-OS [1] (C-Axis Aligned Crystal Oxide Semiconductor)

- Typical example : InGaZnO
- Excellent FET property
  - Extremely low off-state current

I_{off} < 50 yA/μm @85℃
(y = 10^{-24})
Y. Sekine et al, ECS Trans '11

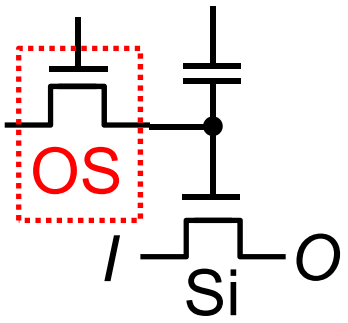
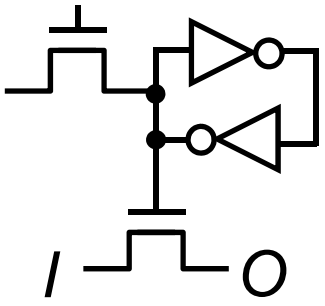
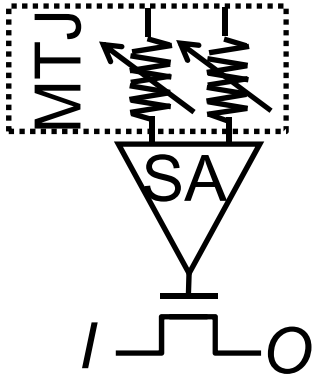
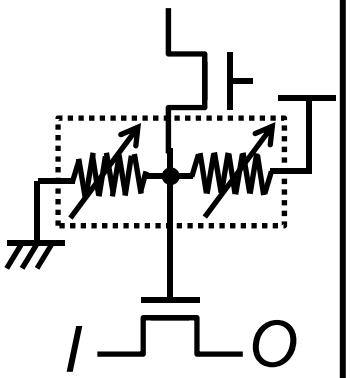
LSI Application featuring Long Data Retention





Background (2/2)

Comparison among **C**onfiguration **M**emories (**CM**)

	CAAC-OS [2]	**SRAM**	**MRAM** [3]	**RRAM** [4]
Circuit (Including Pass Gate)				
Volatile or **N**on**v**olatile	NV	V	NV	NV
Switch Speed	Good	Normal	Normal	Normal
Elements	2Tr.+1C	6Tr.	Many Tr.+2R	2Tr.+2R

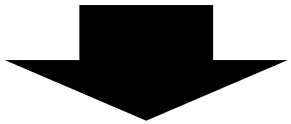
Motivation

Previous work ([5]*SSDM2013*)

Fine-Grained (FG) Power Gating (PG)

with CAAC-OS FPGA

PG is performed in each **P**rogrammable **L**ogic **E**lement (PLE).

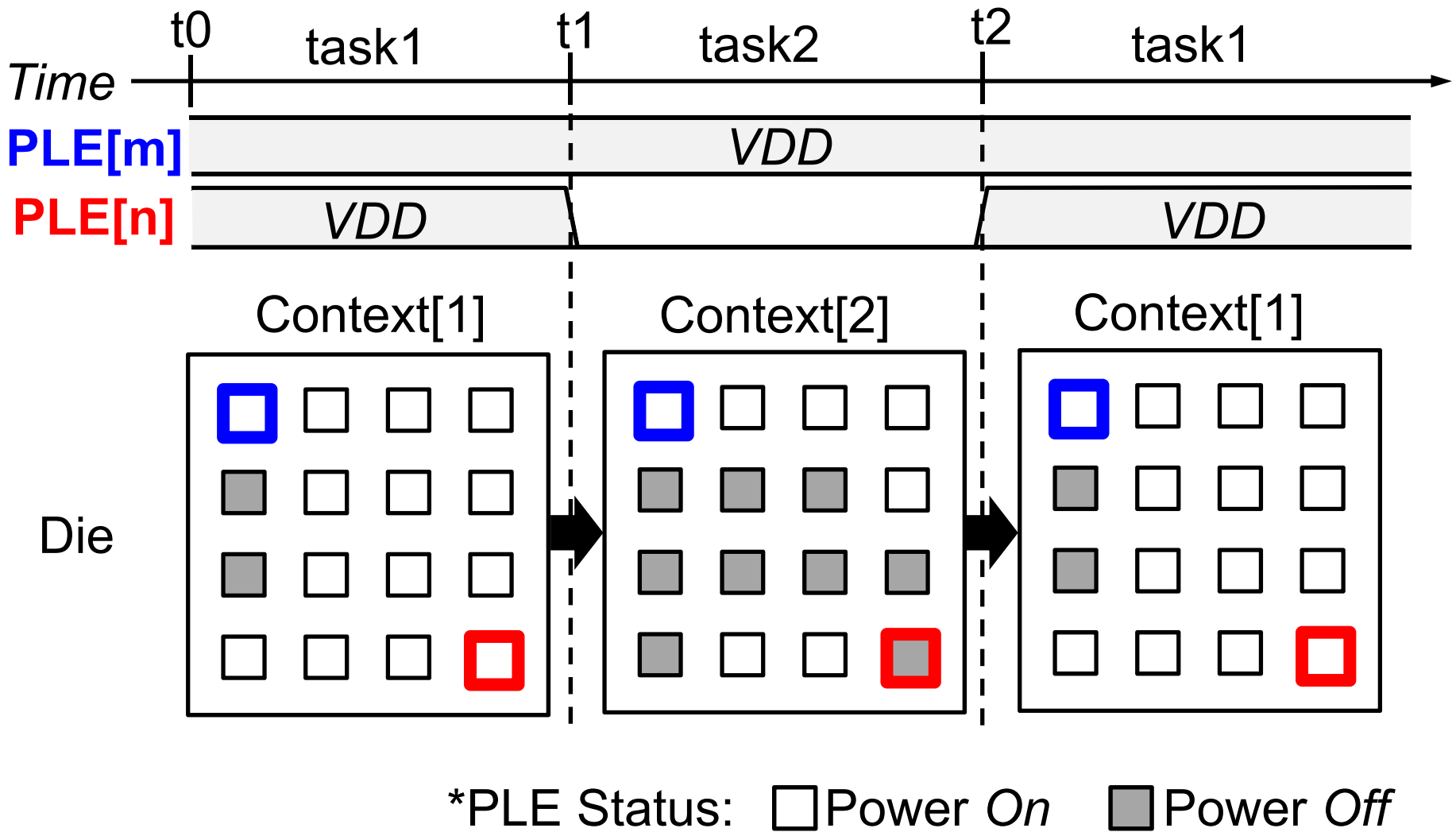


This work

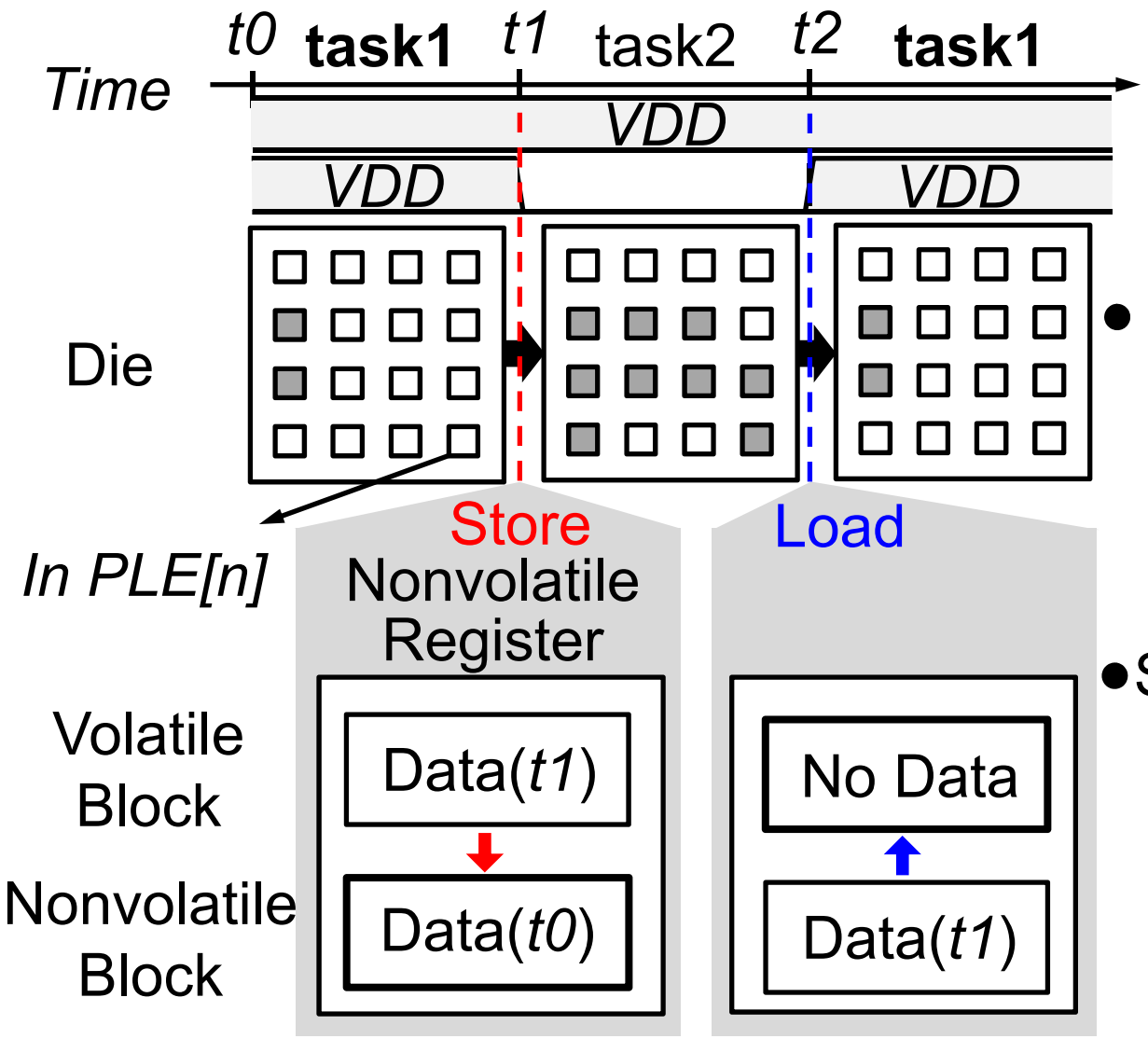
FG Normally-Off (Noff) Computing
with CAAC-OS FPGA Using Nonvolatile Register

Tasks are stopped or resumed based on context switching.
Power is supplied only to PLEs performing actual computation.

Fine-Grained Noff Computing



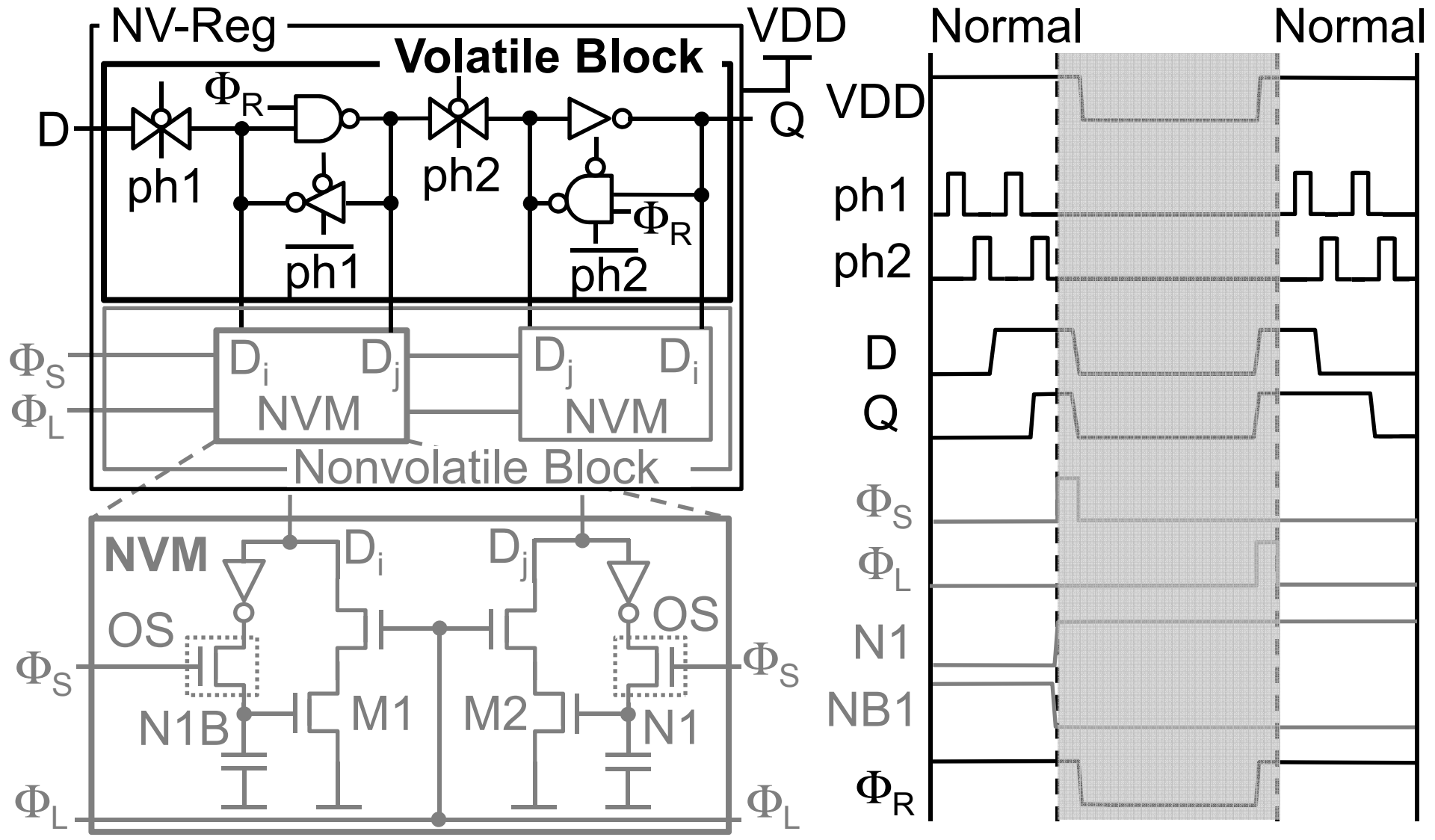
Fine-Grained Noff Computing



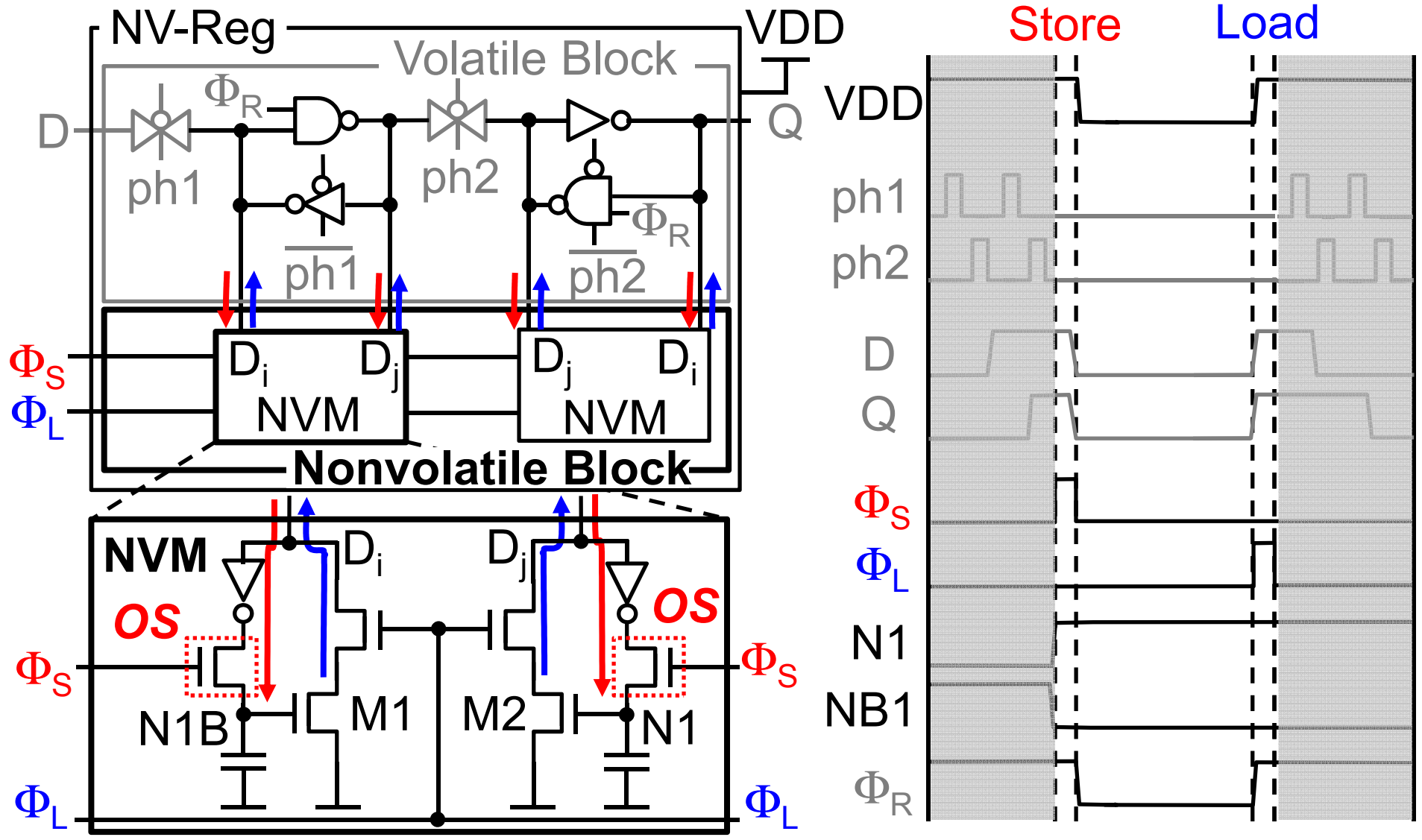
Key Points

- High-speed and Low-power Store to/Load from Nonvolatile Block
- Stable Clock Distribution realized by 2 Phase Non-Overlap Clock Scheme

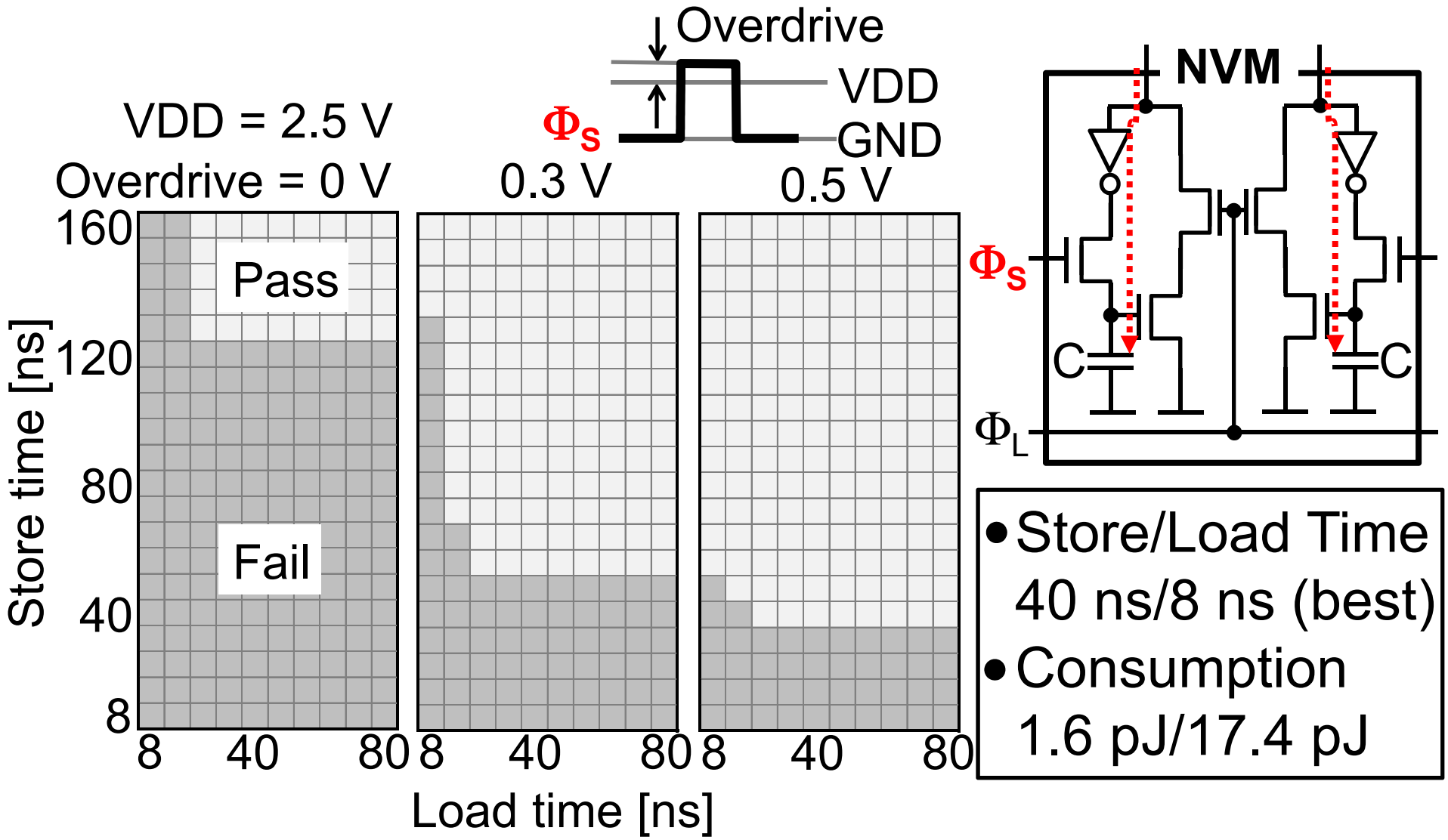
Nonvolatile Register (NV-Reg)



Nonvolatile Register (NV-Reg)

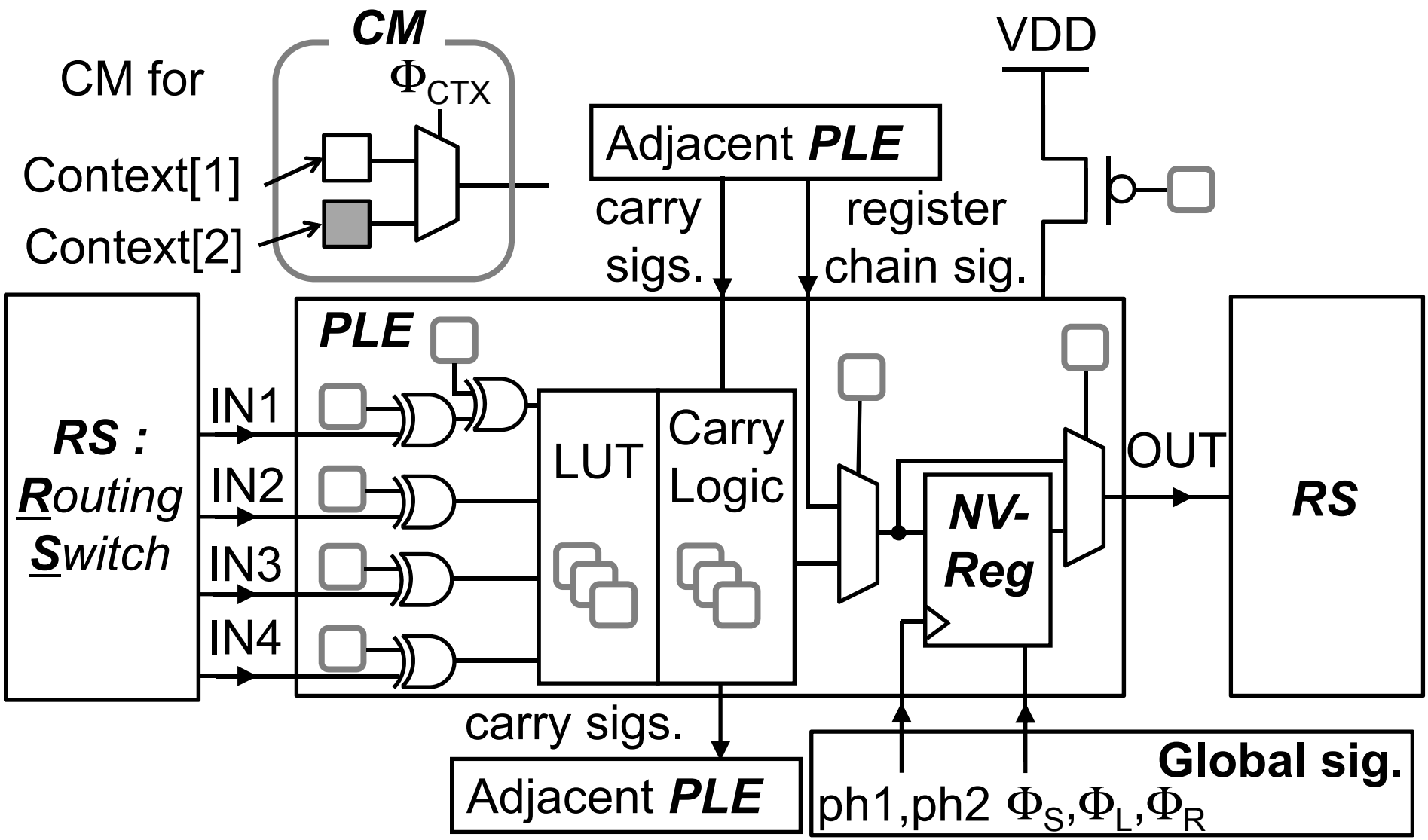


Characteristics of NV-Reg

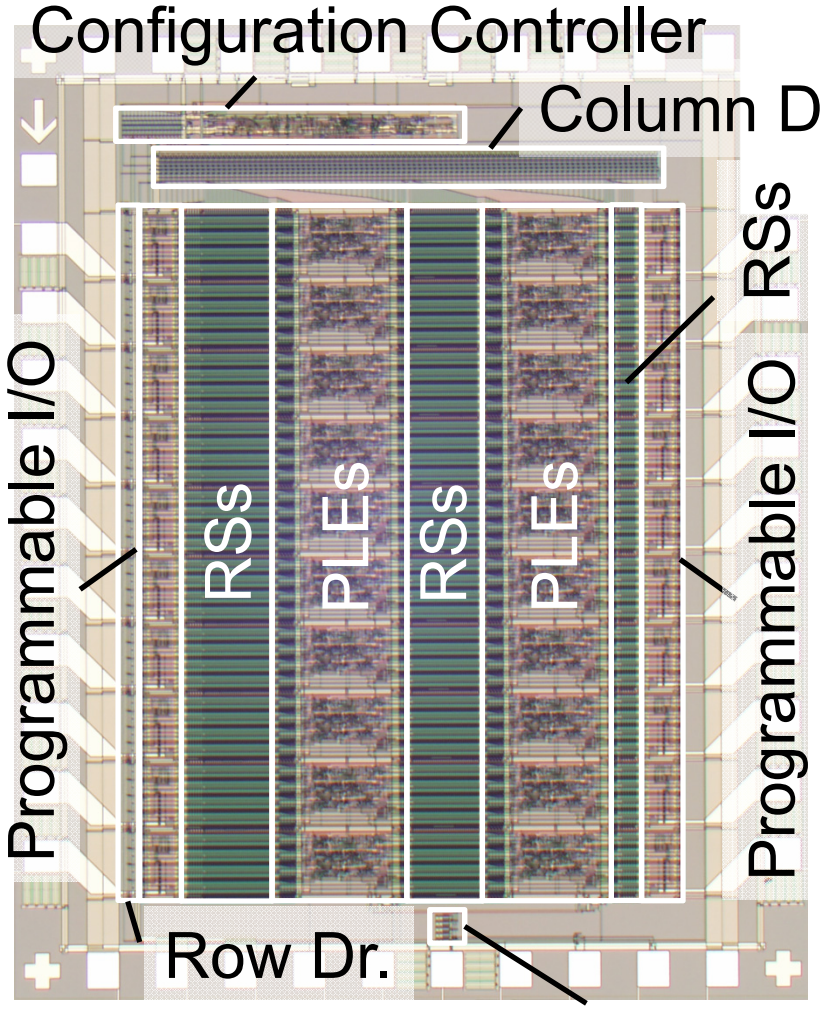


- Store/Load Time
  40 ns/8 ns (best)
- Consumption
  1.6 pJ/17.4 pJ

Block Diagram of Programmable Logic Element (PLE)



Die Photograph



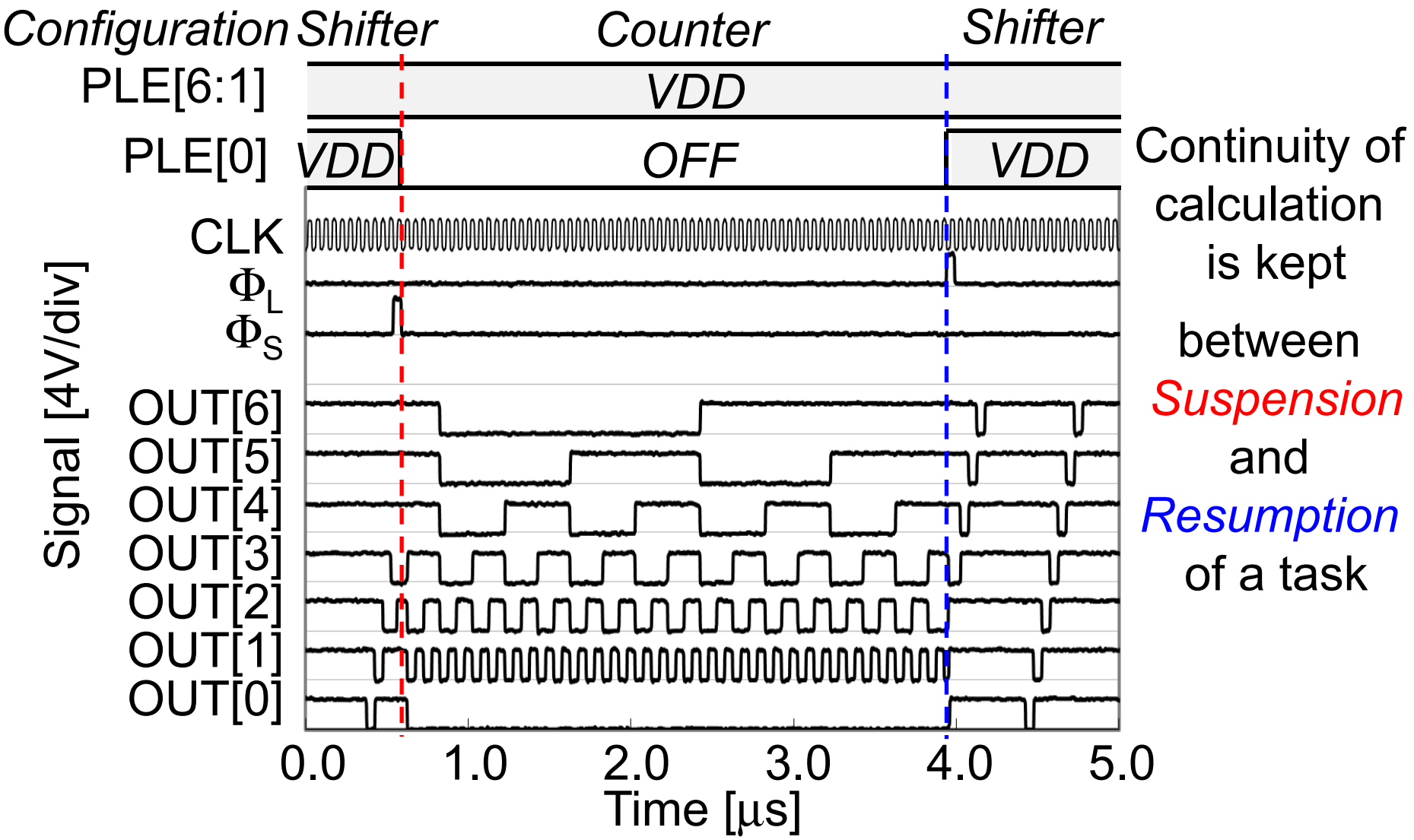
- Hybrid Process

a 1.0-μm CAAC-OS FET
on
a 0.5-μm CMOS FET

- Area Overhead for Adding FG-Noff Function

Register (40%)
PLE (0.6%)
Die (0.3%)

Demonstration of Noff Computing



Continuity of calculation is kept between *Suspension* and *Resumption* of a task

Summary

Fine-Grained Noff Computing is realized by CAAC-OS-based FPGA

Stopping / Resuming task based on context switching
Operation with min. power in each task

- ***NV-Reg*** realizes high-speed data store/load
- *2-phase non-overlap clock scheme*
  enables supply of stable clock signal
- ***Hybrid process*** of CAAC-OS FETs / CMOS FETs

A 1TOPS/W Analog Deep Machine-Learning Engine with Floating-Gate Storage in 0.13μm CMOS

Junjie Lu, Steven Young, Itamar Arel,
and Jeremy Holleman

The University of Tennessee, Knoxville

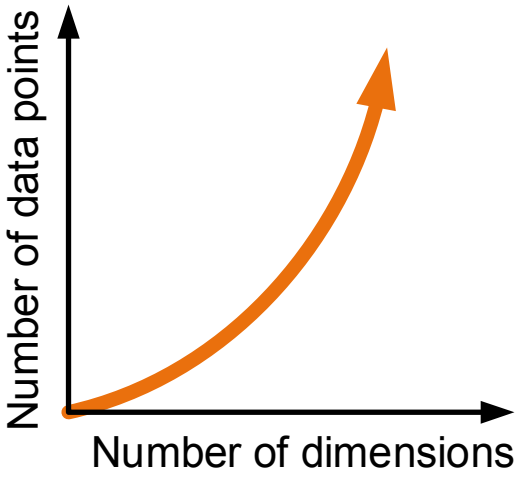
THE UNIVERSITY of TENNESSEE KNOXVILLE

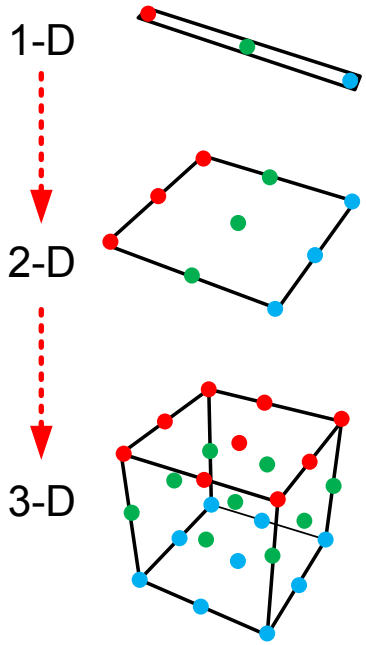
Outline

- Background and motivation
- Architecture and algorithm
- Circuit design
- Measurement results
- Conclusion

The "Curse of Dimensionality" and Deep Machine Learning (DML)

- The difficulty of a machine learning task grows exponentially with the dimension of the input – “Curse of Dimensionality”
- A DML system mimics the hierarchy in the human brain to achieve robust feature extraction





Analog Deep Machine Learning

- DML systems implemented on digital platform – power consumption prohibits energy-constraint application and scaling-up
- Analog signal processing can provide higher efficiency
  - Makes use of computation primitives in device/physics
  - Multi-bit encoding of information
  - But more sensitive to noise and mismatch

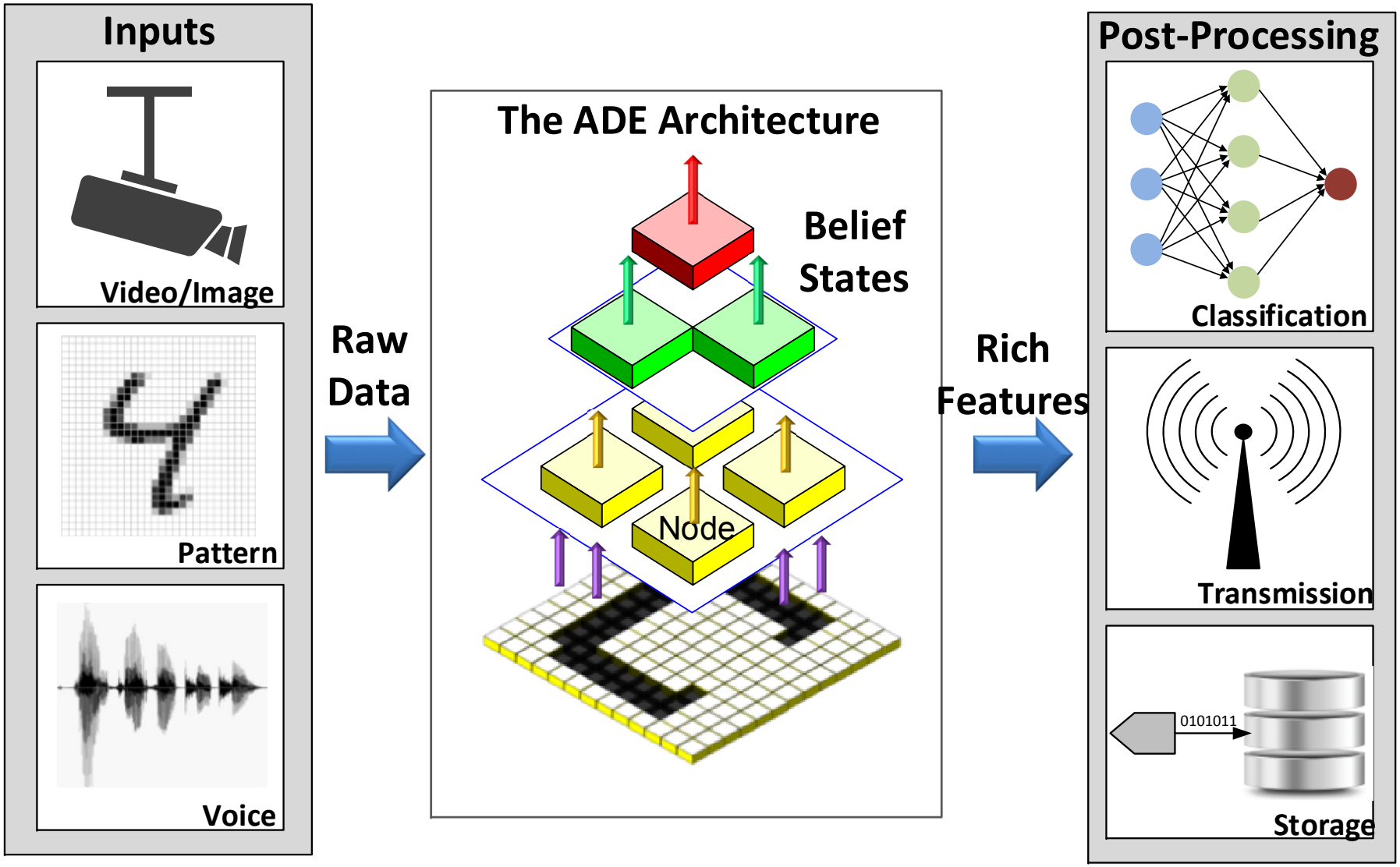
Analog Deep Machine Learning

- An analog DML engine (ADE)
  - Implementing DeSTIN
  - Featuring online unsupervised trainability
  - Non-volatile memory
  - Facilitating autonomous operation with intermittent power
  - Peak energy efficiency of 1TOPS/W
  - Algorithm level feedback desensitizes the system to circuit imperfections

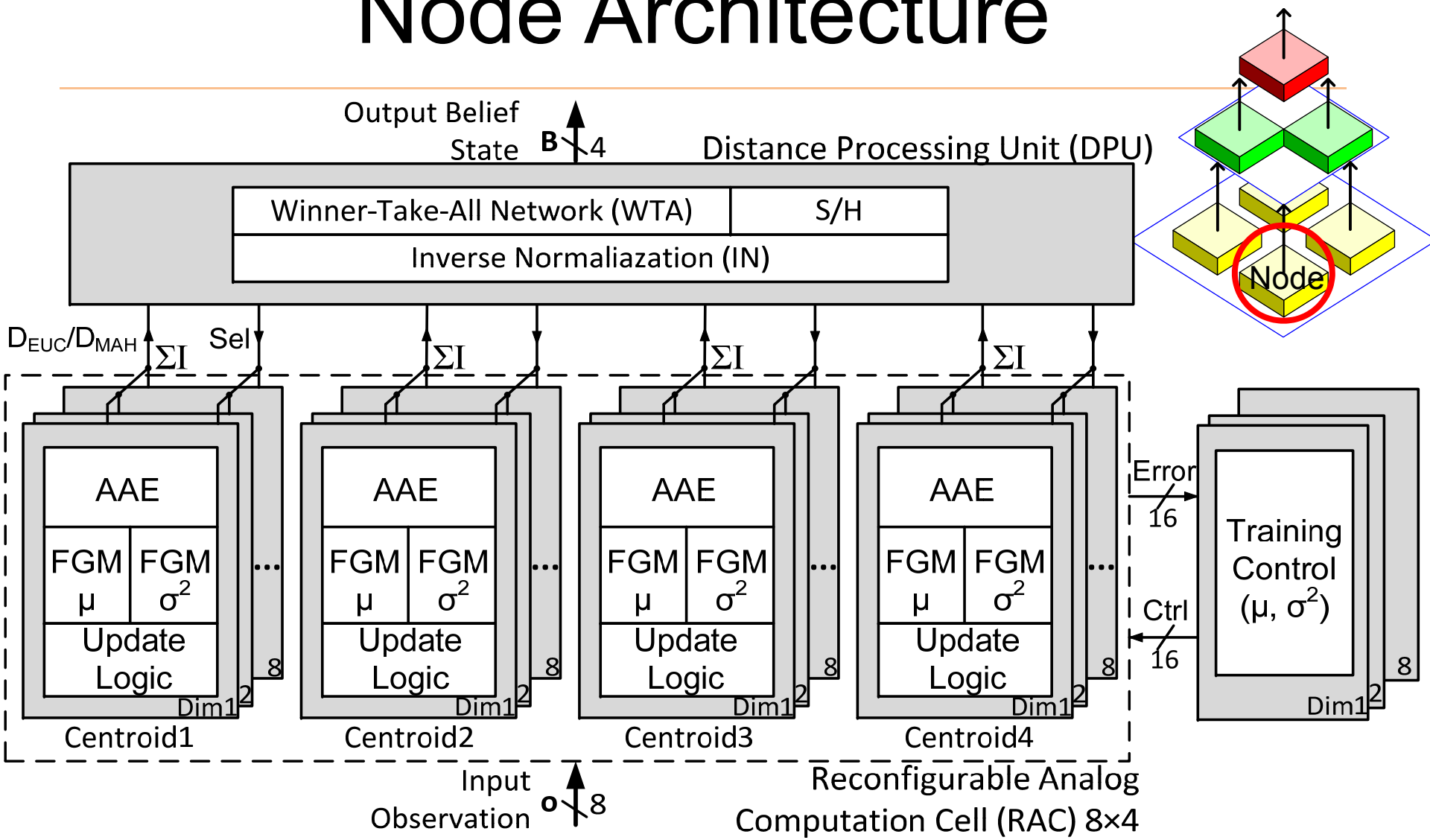
Outline

- Background and motivation
- Architecture and algorithm
  - System Architecture
  - Node Architecture
  - Algorithm
  - System-Level Power Management
- Circuit design
- Measurement results
- Conclusion

System Architecture

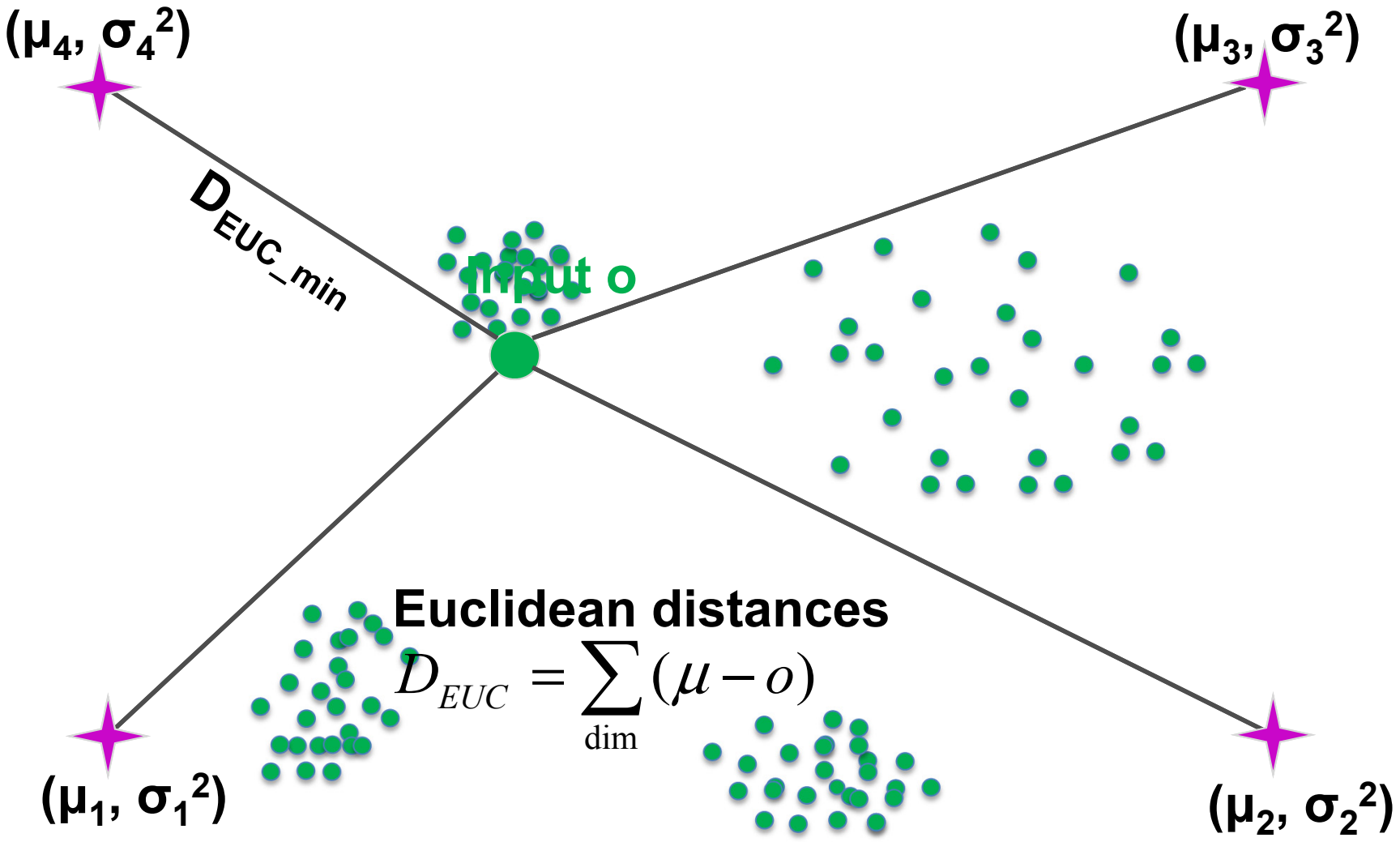


Node Architecture

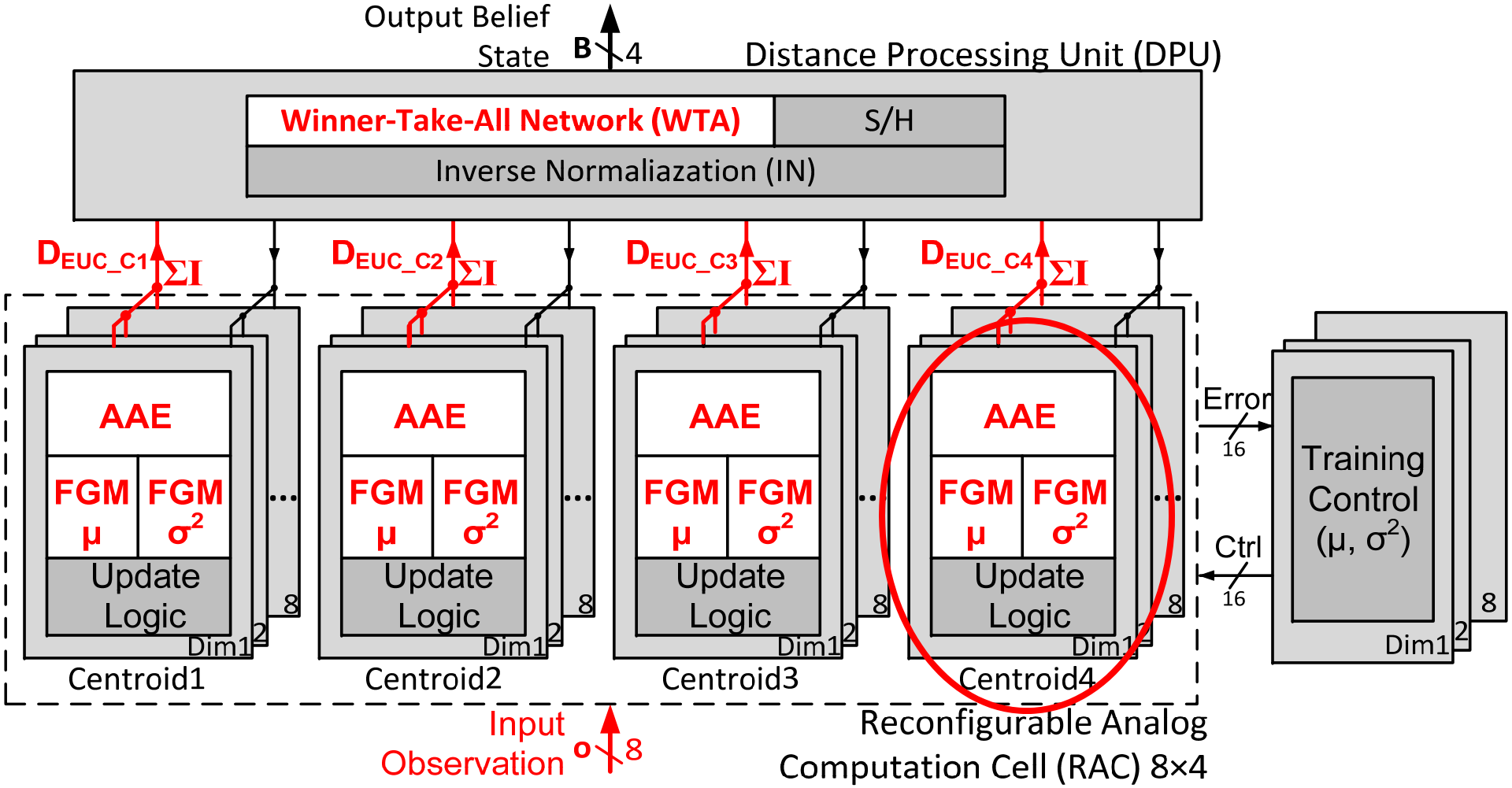


- AAE: analog arithmetic elements
- FGM: floating gate memory

Algorithm – Classification

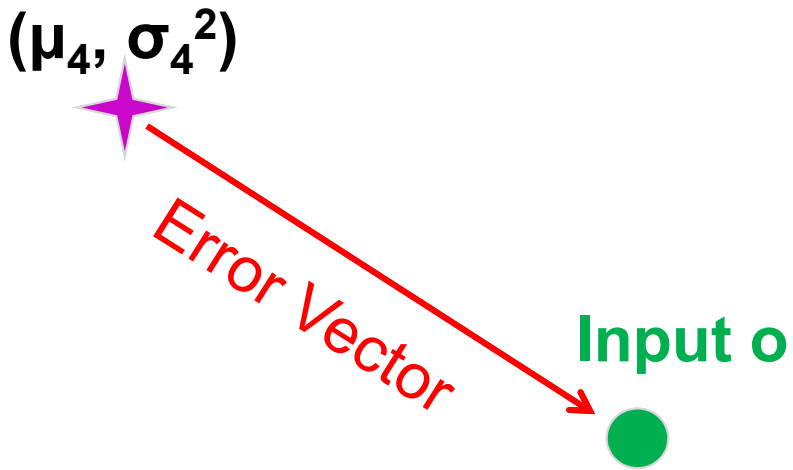


Algorithm – Classification

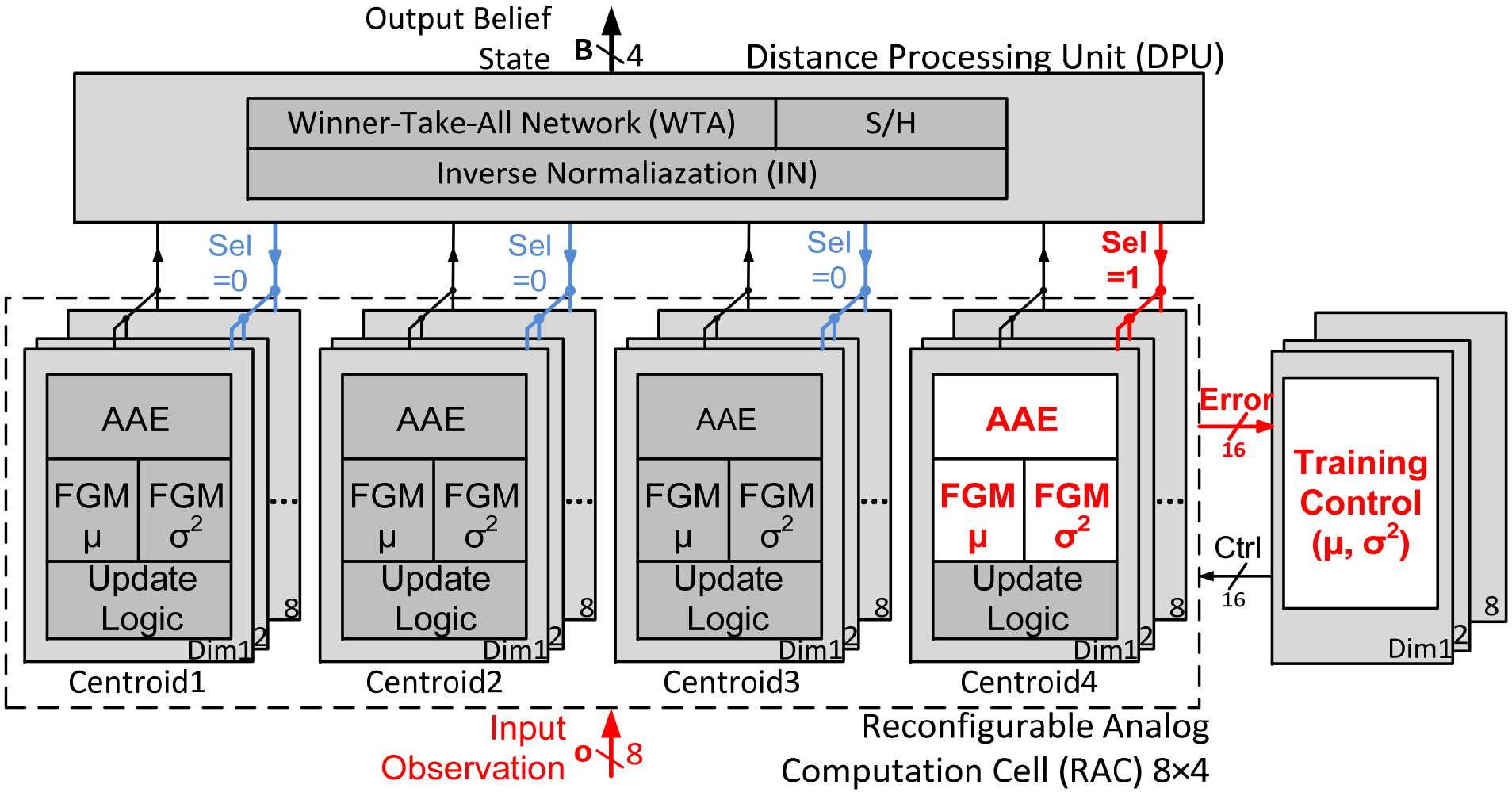


- AAE: analog arithmetic elements
- FGM: floating gate memory

Algorithm – Training Load

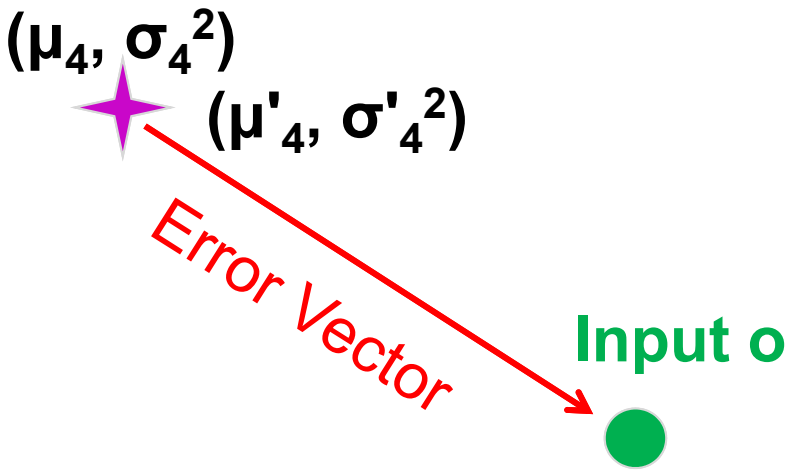


Algorithm – Training Load

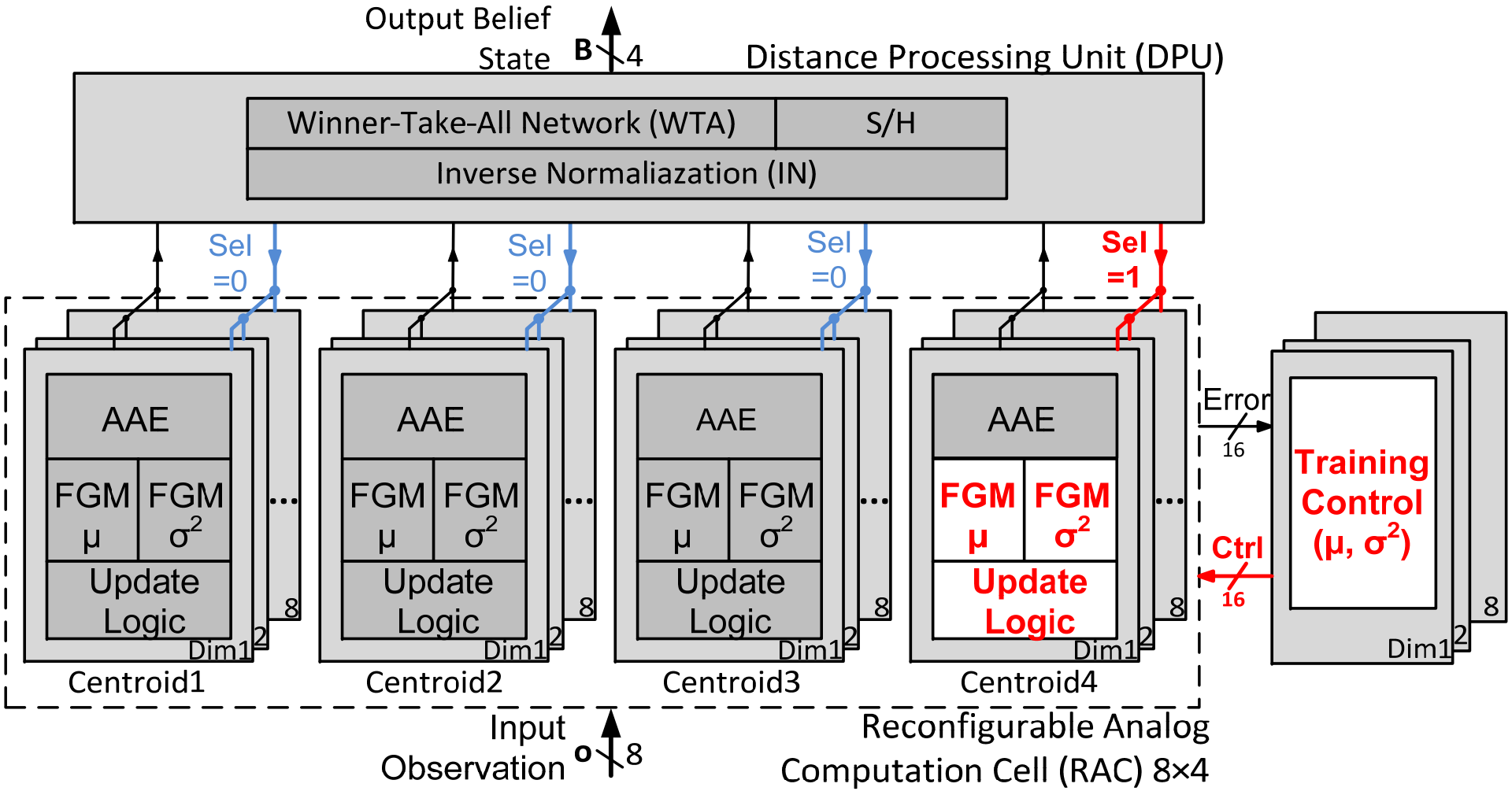


- AAE: analog arithmetic elements
- FGM: floating gate memory

Algorithm – Memory Writing

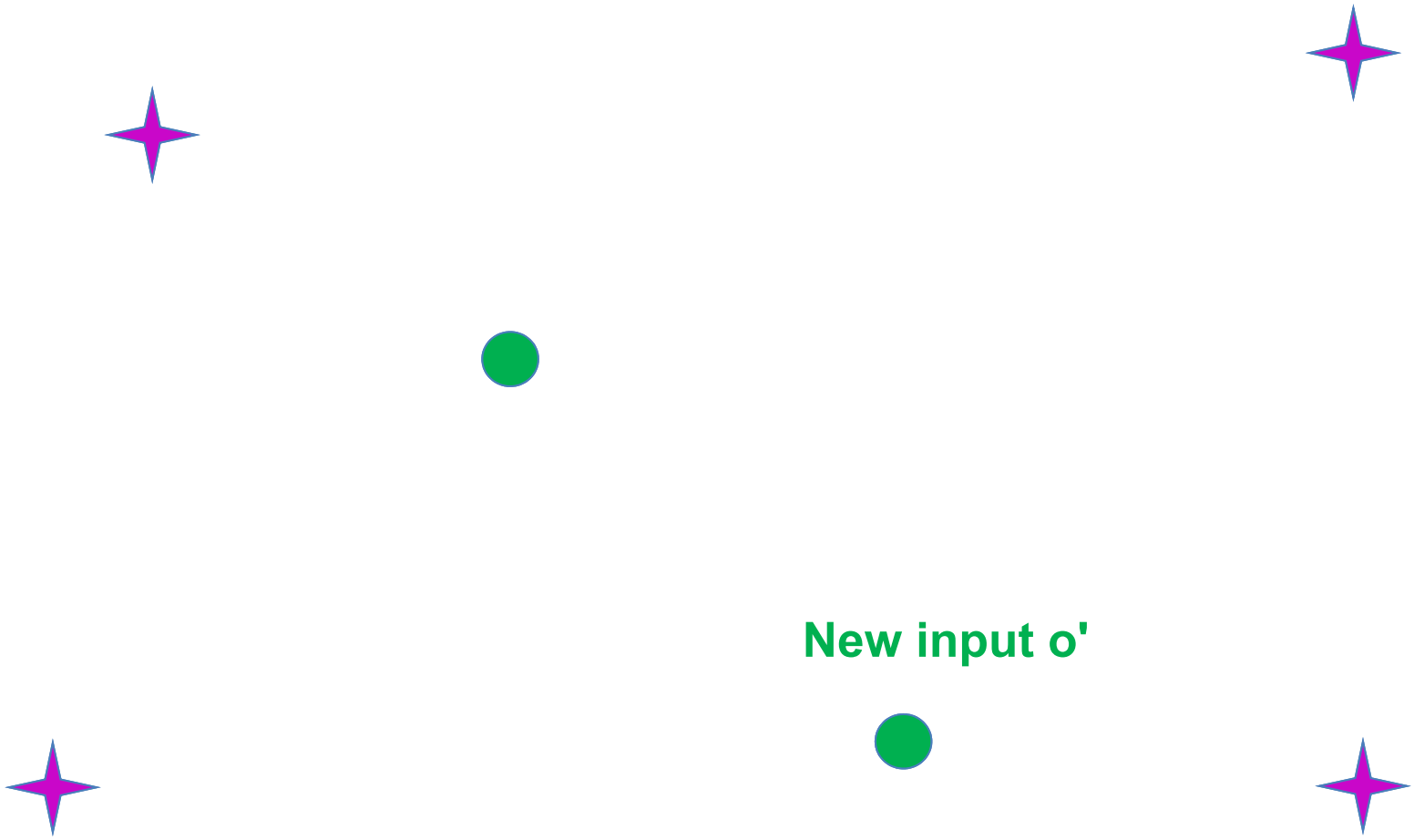


Algorithm – Memory Writing

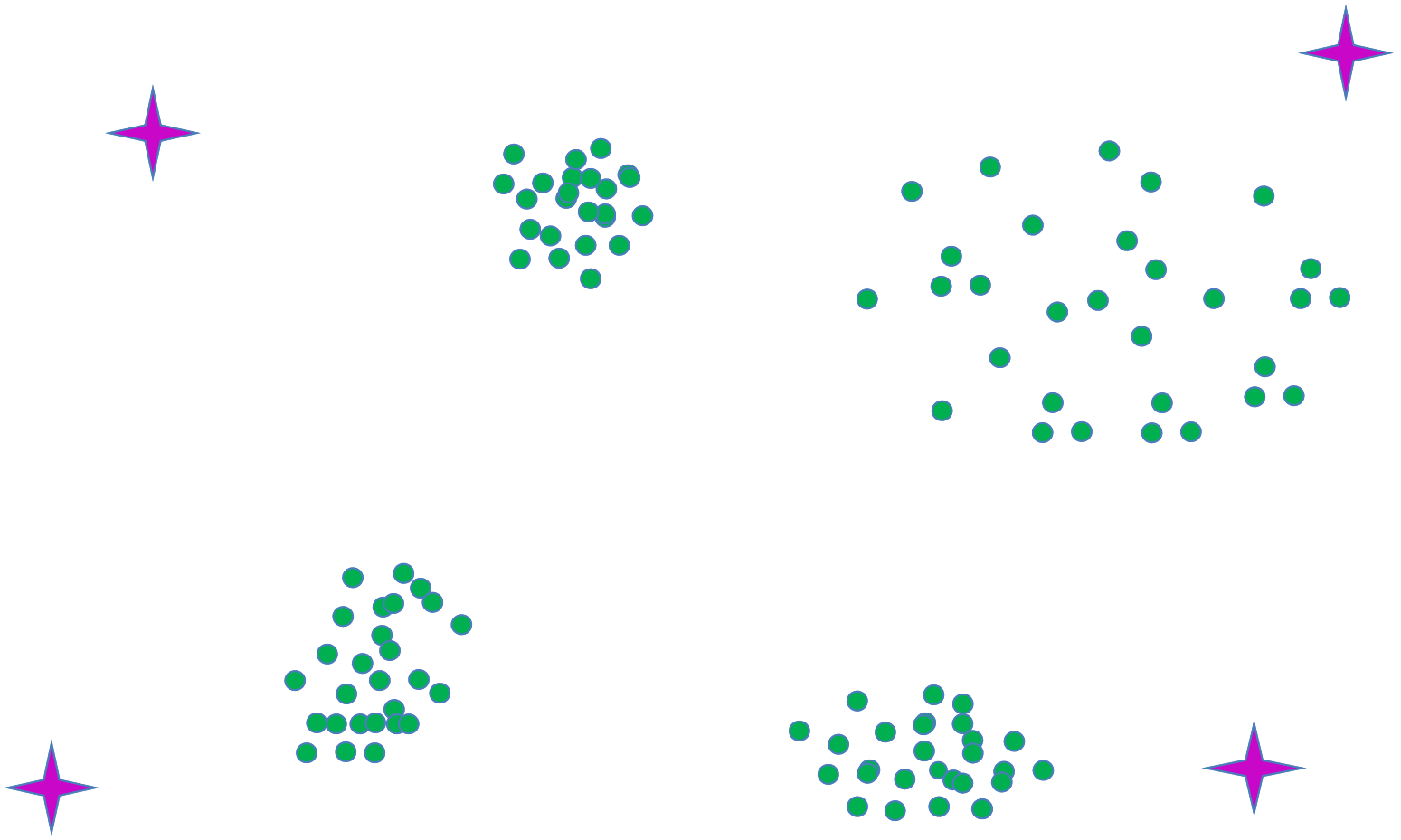


- AAE: analog arithmetic elements
- FGM: floating gate memory

Algorithm – Next Cycle



Algorithm – Convergence

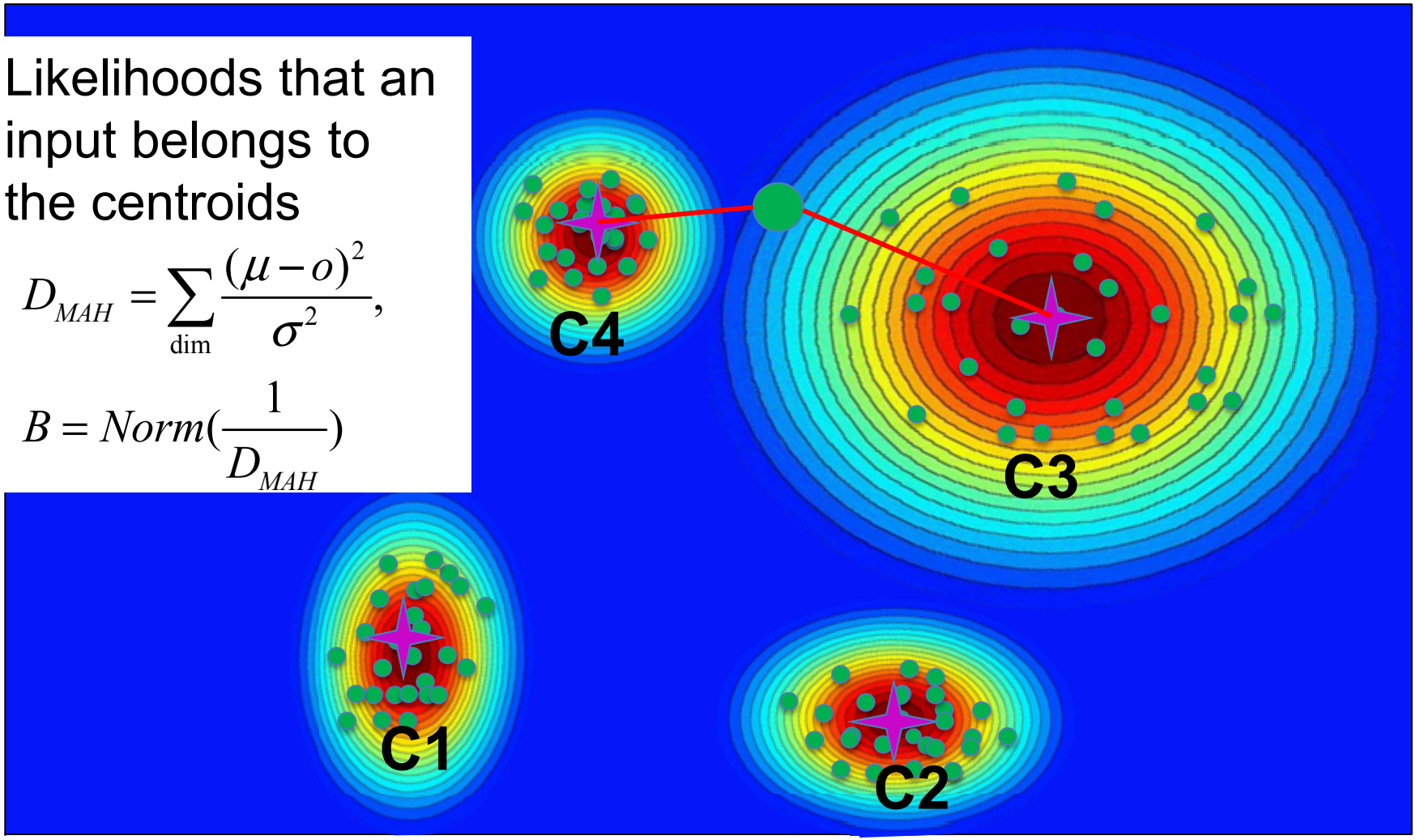


Algorithm – Belief Construction

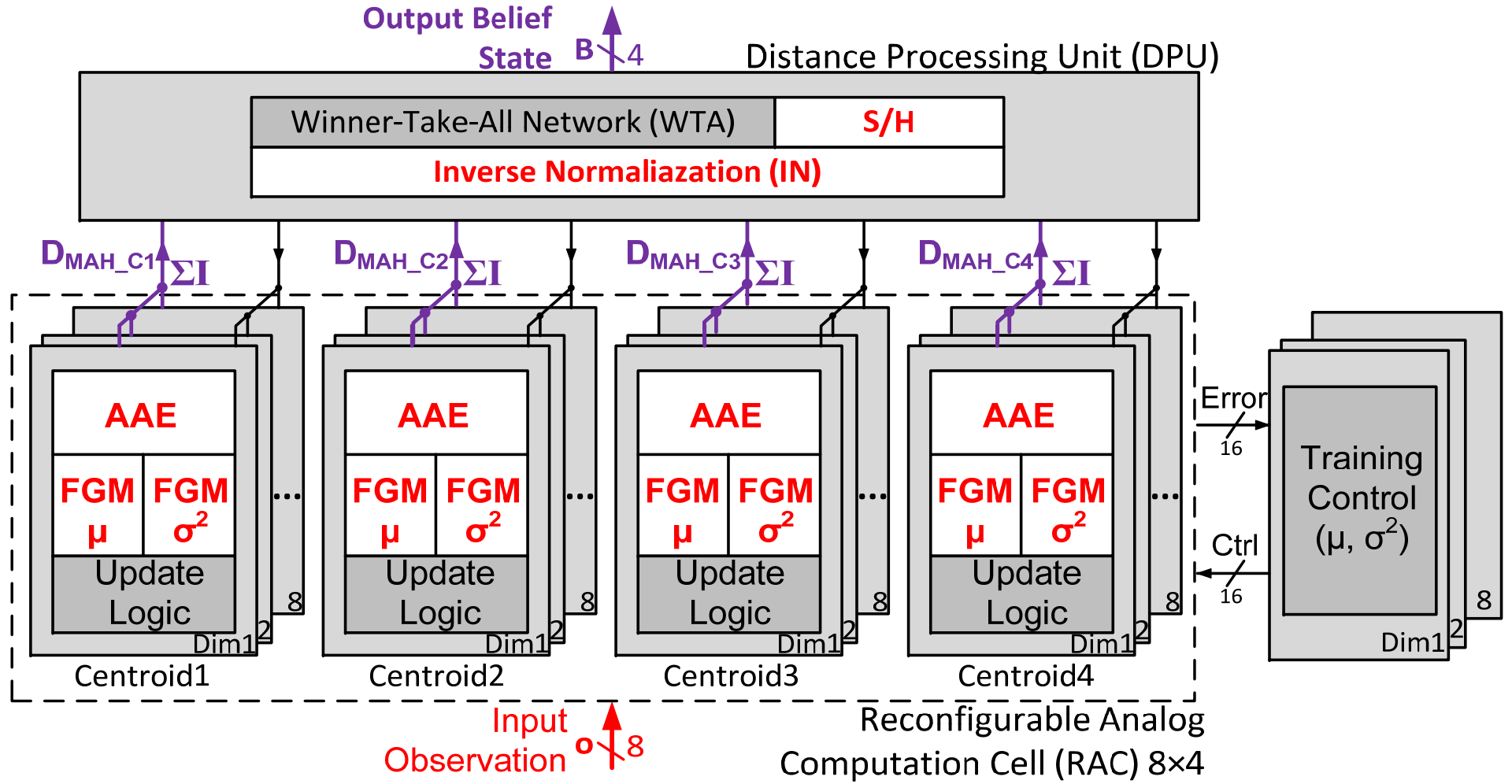
Likelihoods that an input belongs to the centroids

$$D_{MAH} = \sum_{\dim} \frac{(\mu - o)^2}{\sigma^2},$$

$$B = Norm(\frac{1}{D_{MAH}})$$



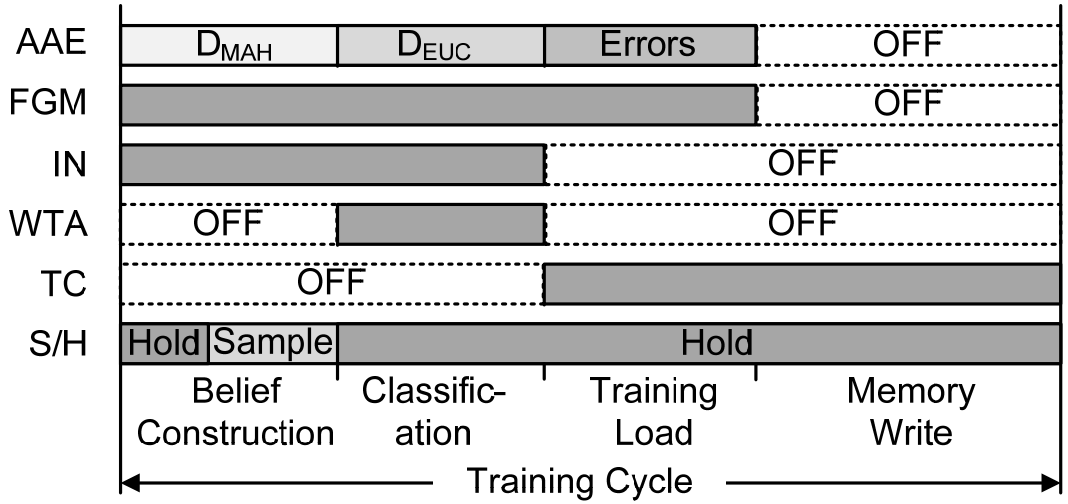
Algorithm – Belief Construction

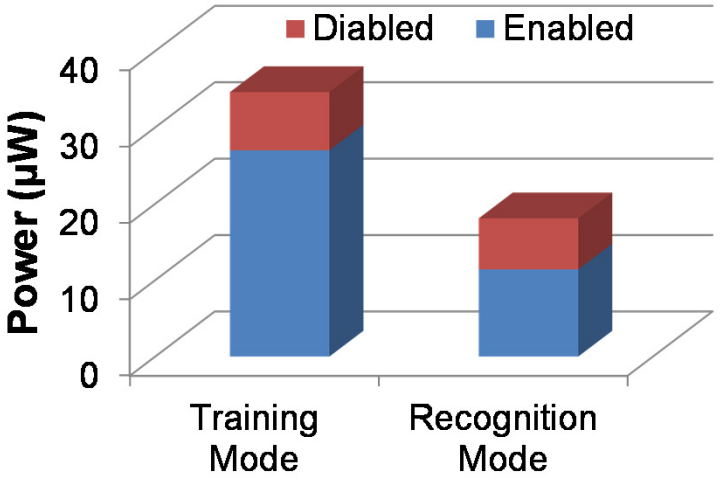


- AAE: analog arithmetic elements
- FGM: floating gate memory

Intra-Cycle Power Gating

- Save power by disabling the inactive circuits
- 22% power saving in training mode
- 37% power saving in recognition mode (memory not updated)

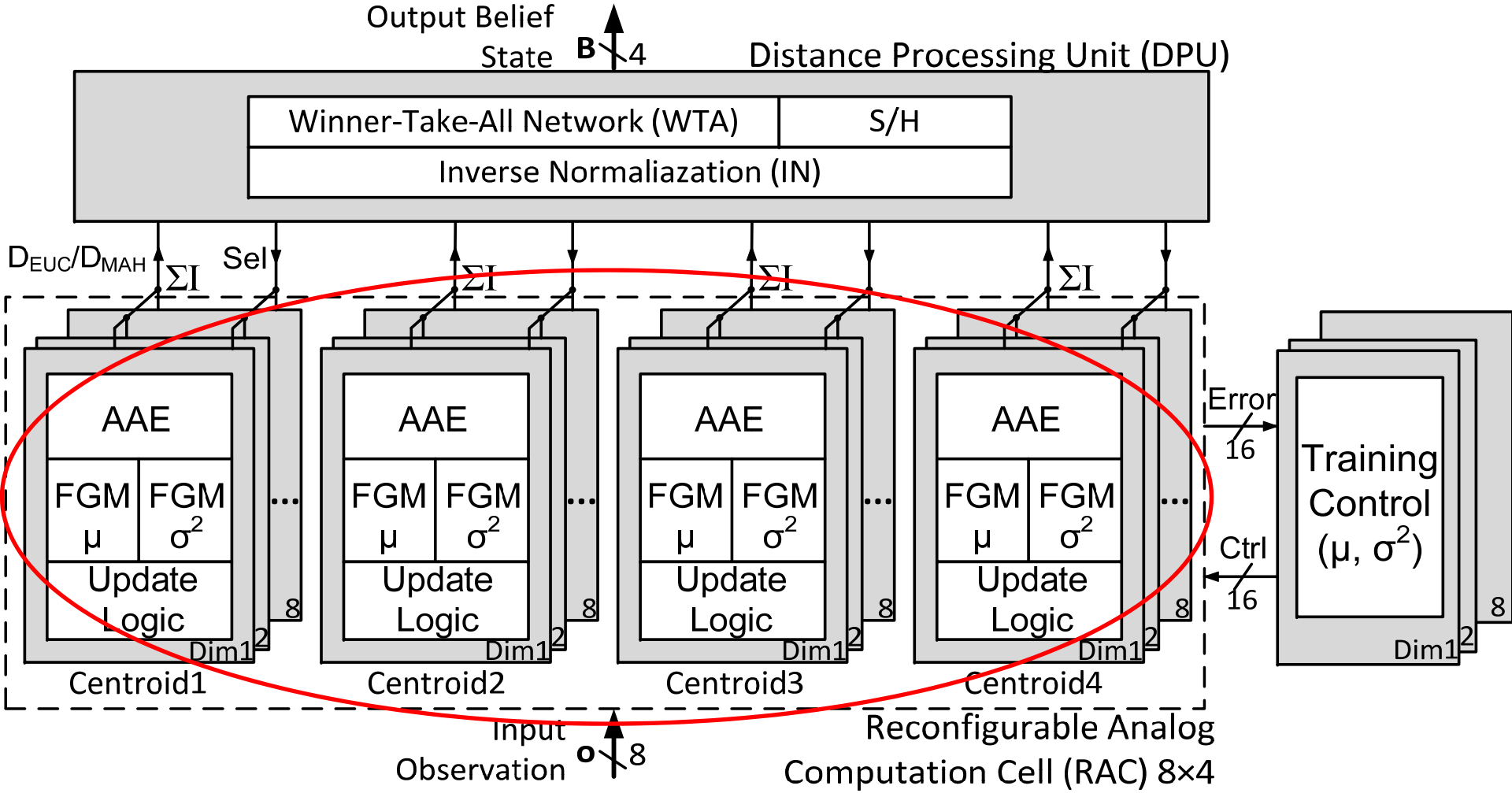




Outline

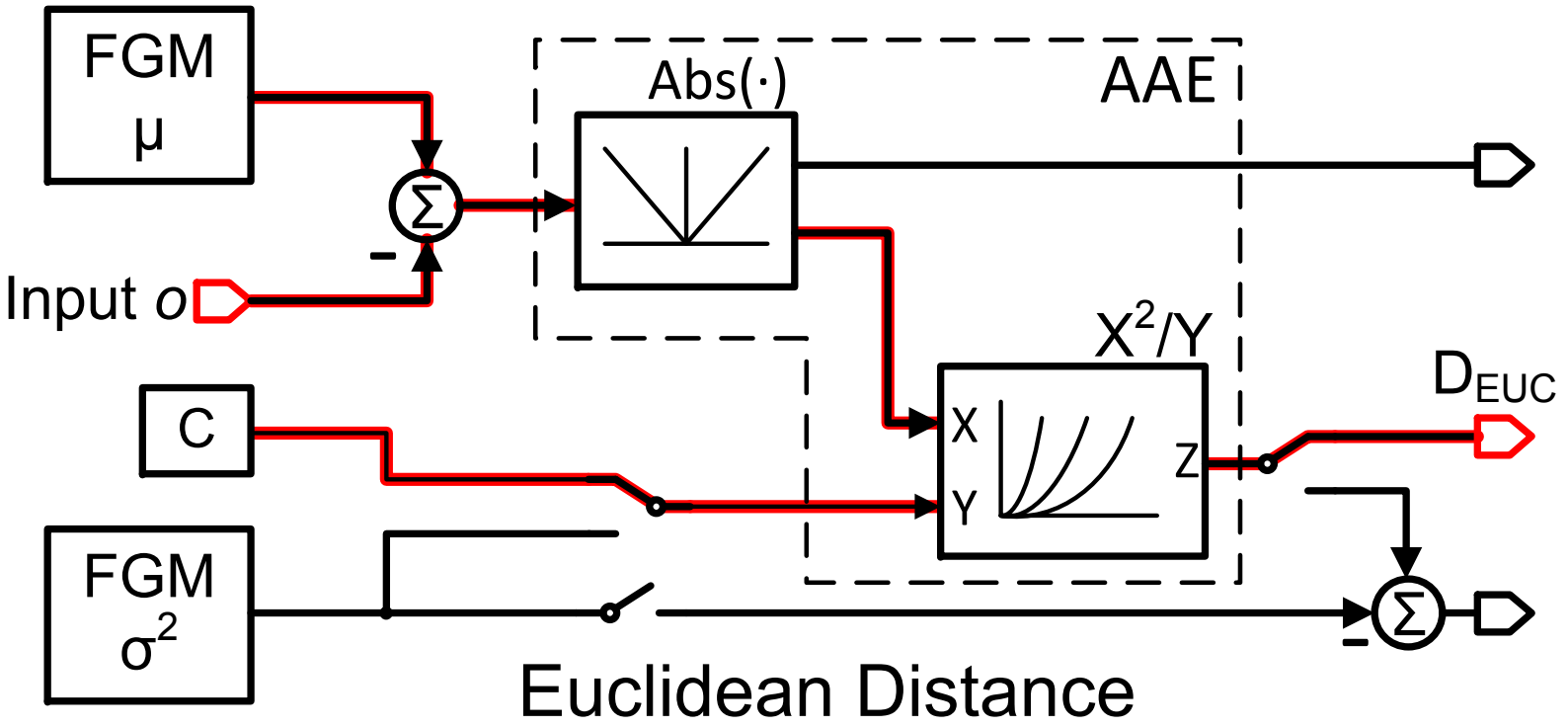
- Background and motivation
- Architecture and algorithm
- Circuit design
  - Reconfigurable Analog Computation
  - Distance Processing
  - Training Control
- Measurement results
- Conclusion

Reconfigurable Analog Computation (RAC)



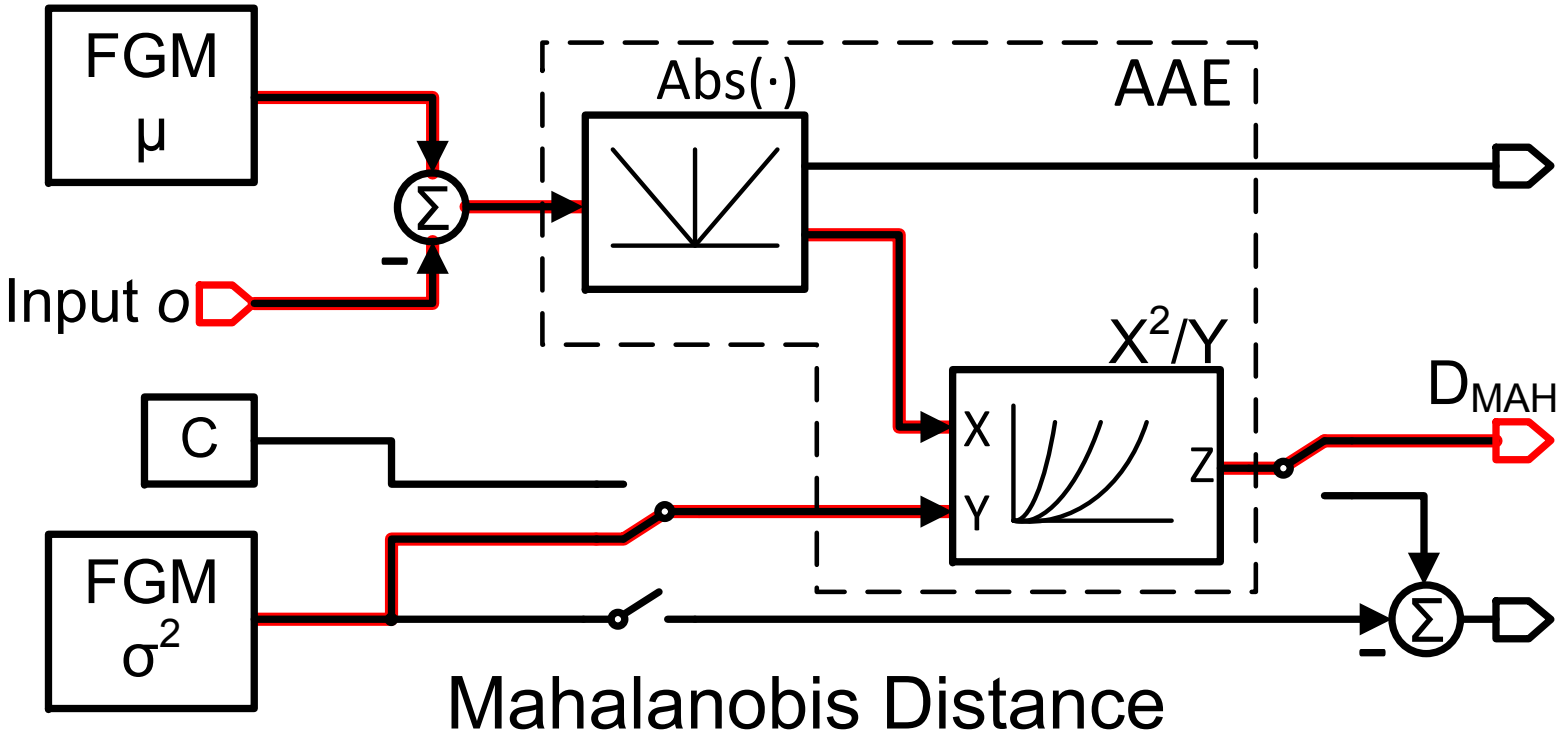
- AAE: analog arithmetic elements
- FGM: floating gate memory

Reconfigurable Analog Computation



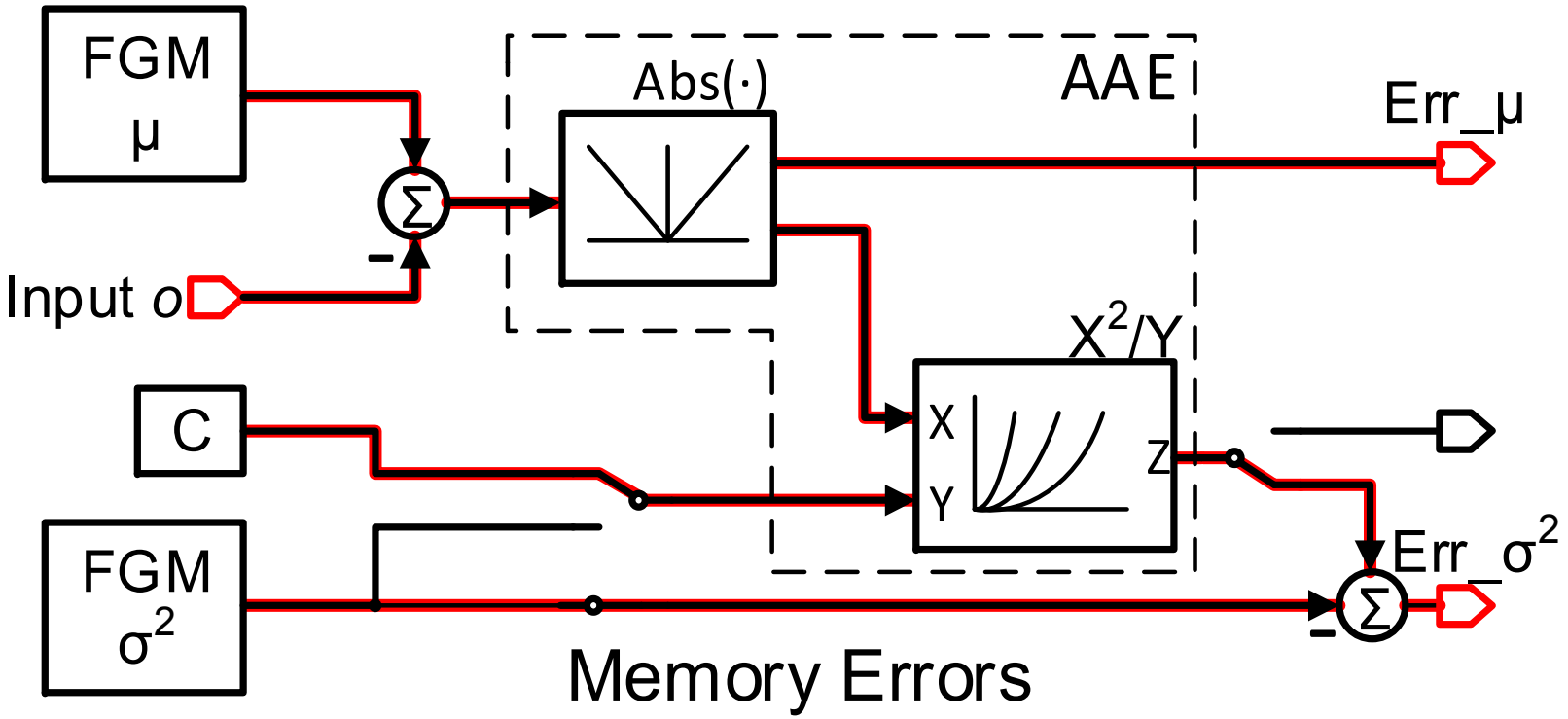
$$D_{EUC} = \sum C^{-1}(o-\hat{\mu})^2,\ \text{C is constant}$$

Reconfigurable Analog Computation



$$D_{MAH} = \sum \frac{(o - \hat{\mu})^2}{\hat{\sigma}^2}$$

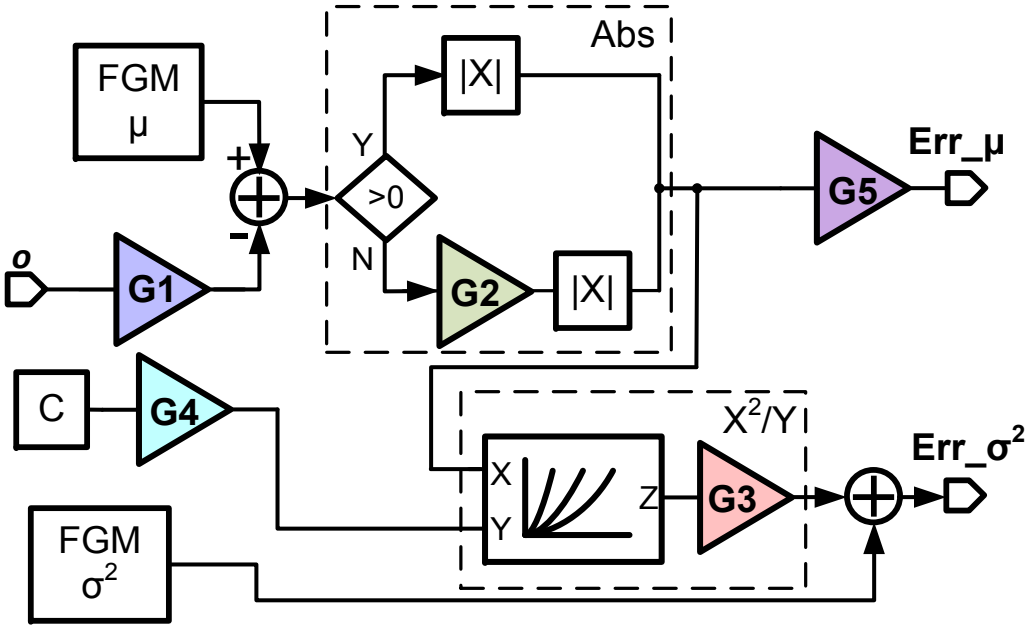
Reconfigurable Analog Computation

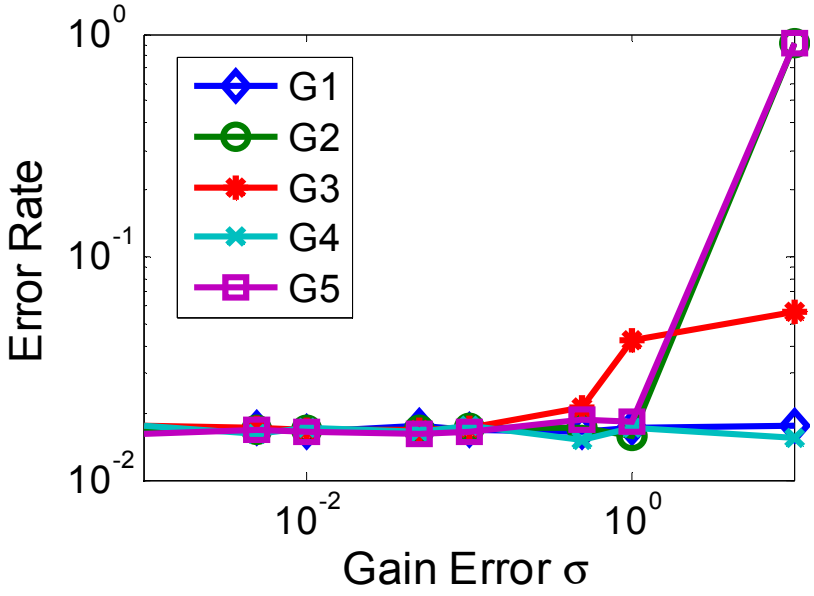


$$\begin{cases} Err_{\mu} = o - \hat{\mu} \\ Err_{\sigma^2} = C^{-1}(o - \hat{\mu})^2 - \hat{\sigma}^2 \end{cases}$$

Transistor Size Scaling

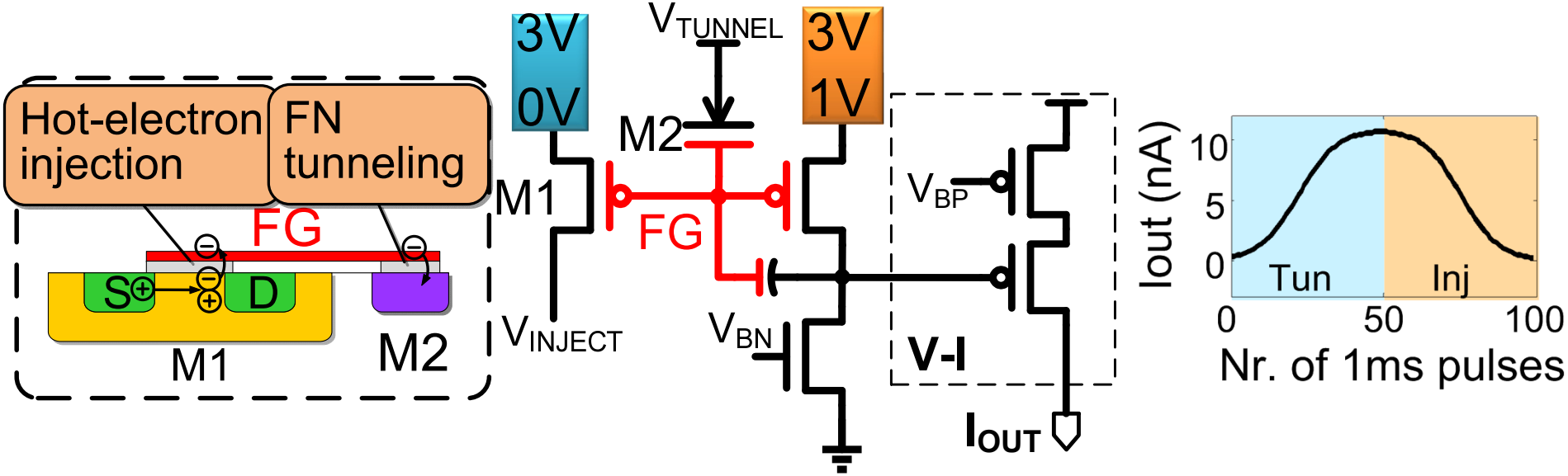
- Robustness to static error inherent in learning algorithm allows aggressive device size reduction
- System modeling and simulation provides knowledge of the system's tolerance to mismatch errors





Floating Gate Analog Memory

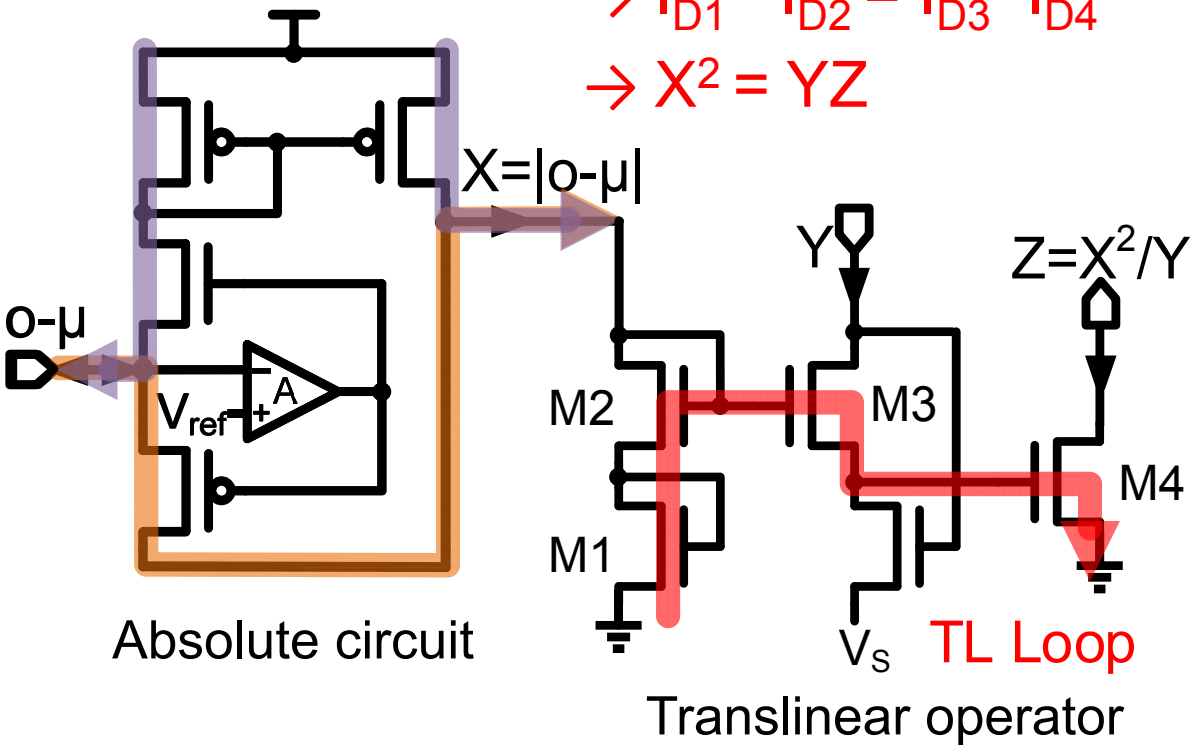
- Capacitive feedback fixes V_{FG} for PW controlled update
- Achieves random-accessible bi-directional update without on-chip charge pump or high-voltage switch
- 2-T VI converter provides current output

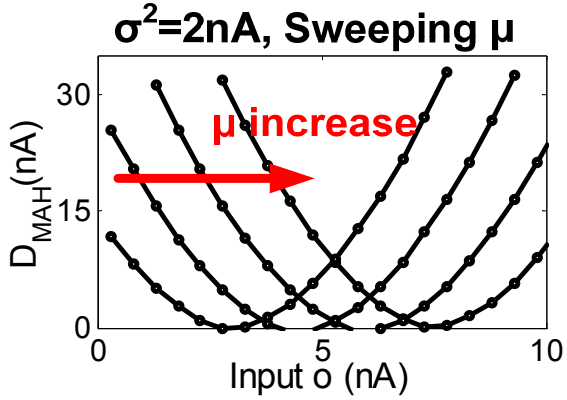


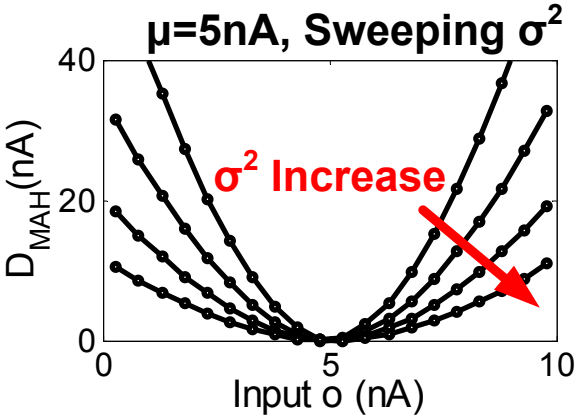
Analog Arithmetic Element

- Absolute circuit rectifies the difference current *o-μ*
- Translinear operator implements efficient X^2/Y function

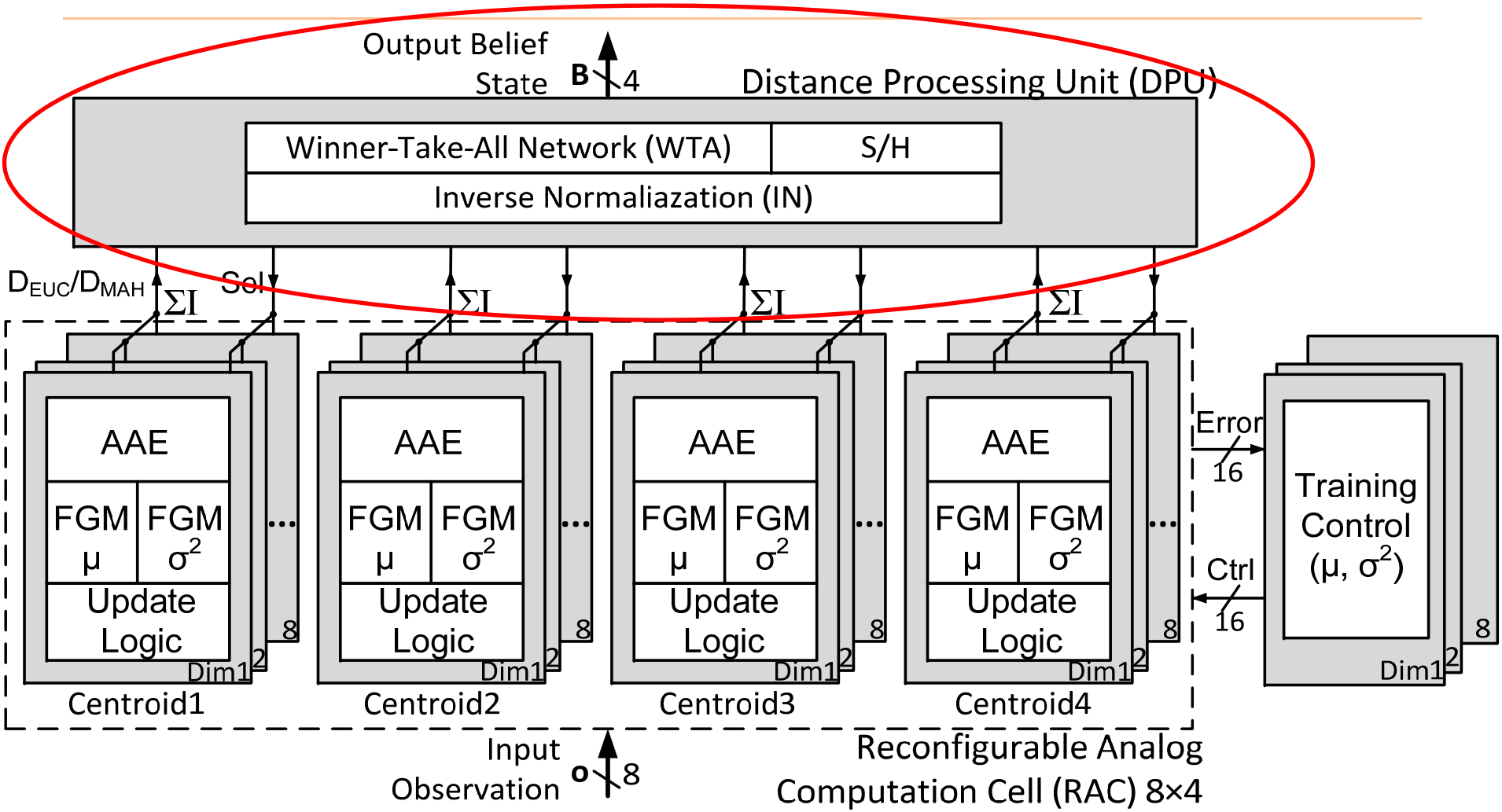
$$V_{GS1}+V_{GS2} = V_{GS3}+V_{GS4}$$
$$\rightarrow I_{D1} \cdot I_{D2} = I_{D3} \cdot I_{D4}$$
$$\rightarrow X^2 = YZ$$







Distance Processing Unit



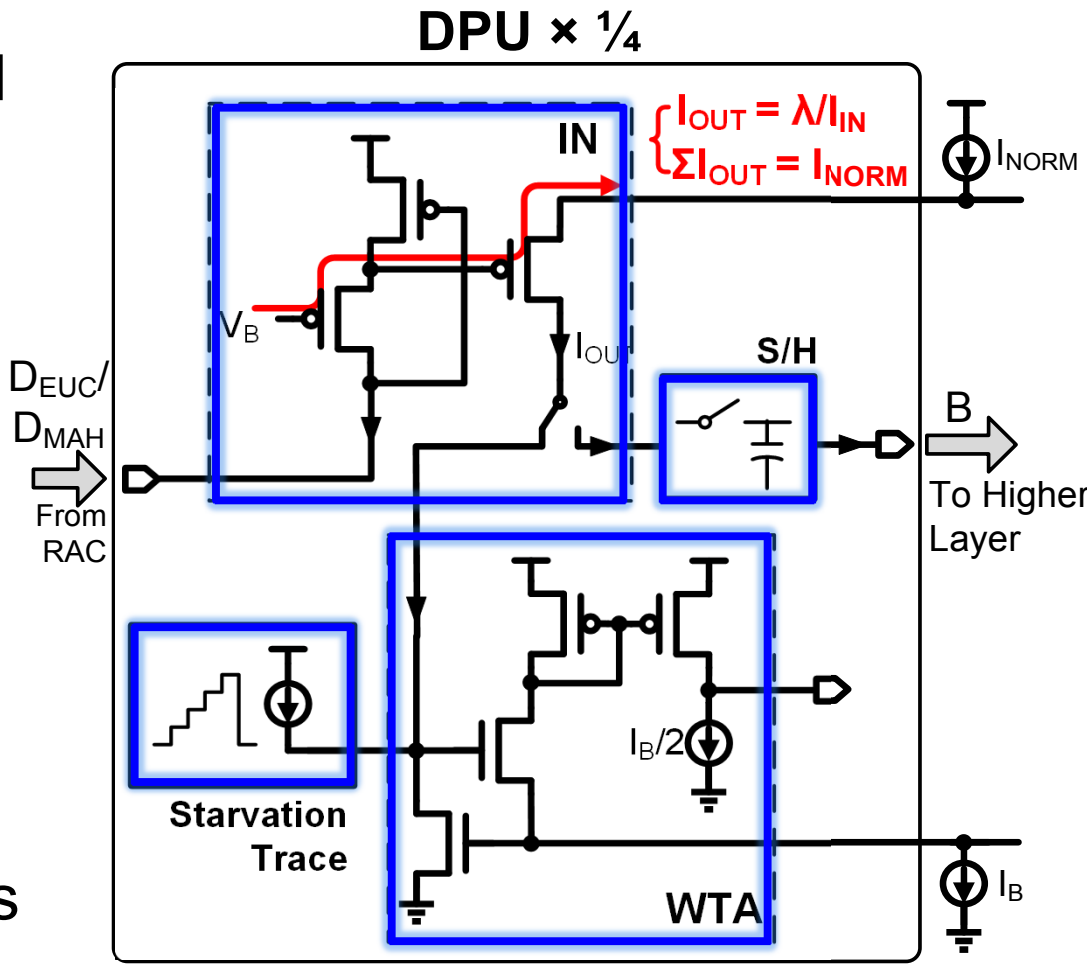
- AAE: analog arithmetic elements
- FGM: floating gate memory

Distance Processing Unit

- IN converts D_{MAH} to valid probability distribution ***B***

$$B = Norm(\frac{1}{D_{MAH}})$$

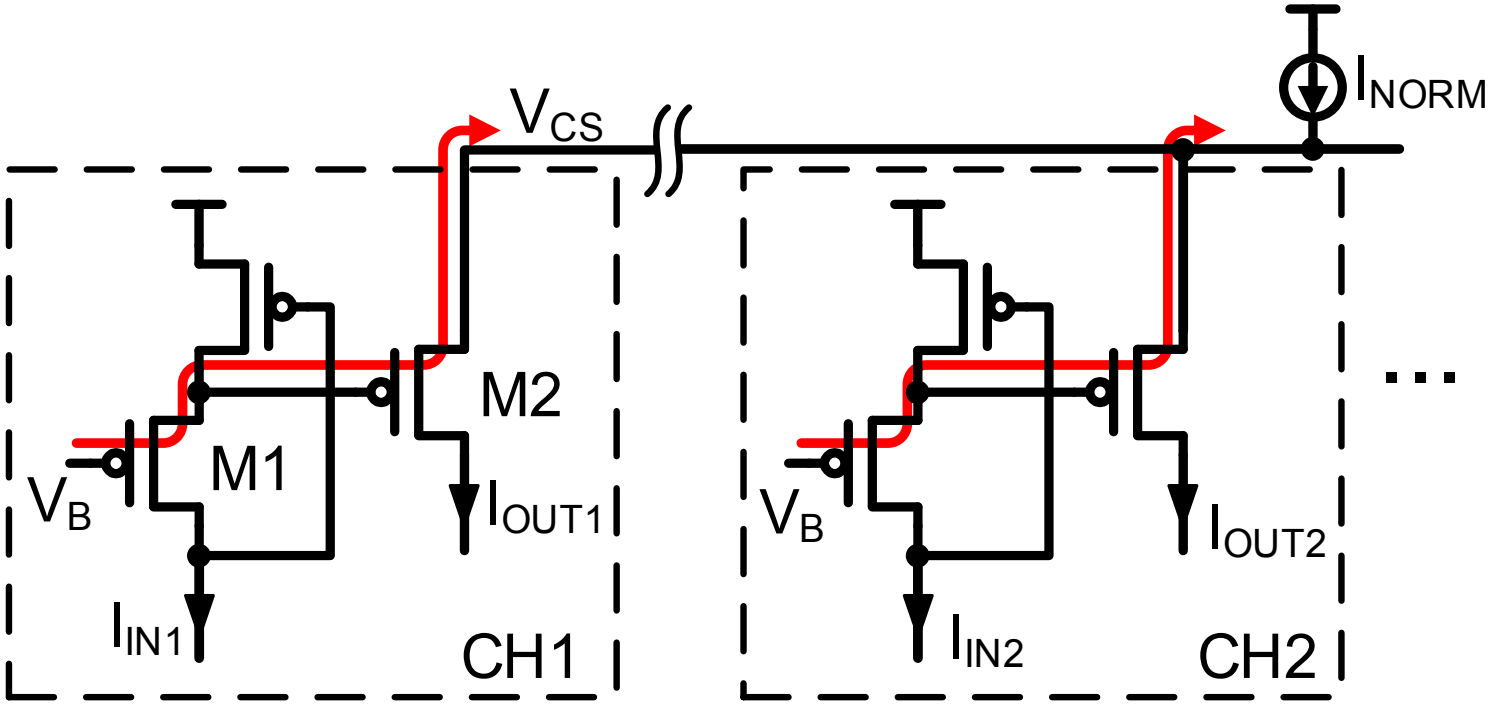
- WTA searches for D_{EUC_min}
- Starvation trace addresses unfavorable initial condition
- S/H enables pipelined operation of all the layers



Inverse Normalization Circuit

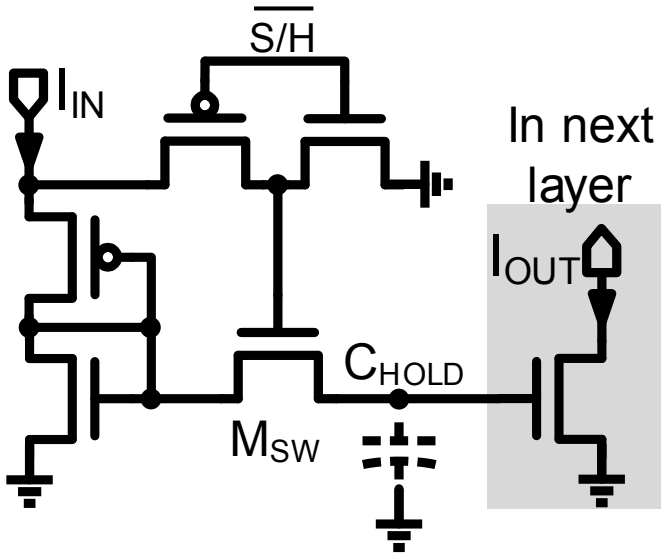
$$I_{IN} \cdot I_{OUT} = I_0^2 e^{\frac{\kappa V_{SG1}}{U_T} + \frac{\kappa V_{SG2}}{U_T}} = I_0^2 e^{\frac{\kappa (V_{CS} - V_B)}{U_T}} = \lambda \Rightarrow I_{OUT} = \frac{\lambda}{I_{IN}}$$

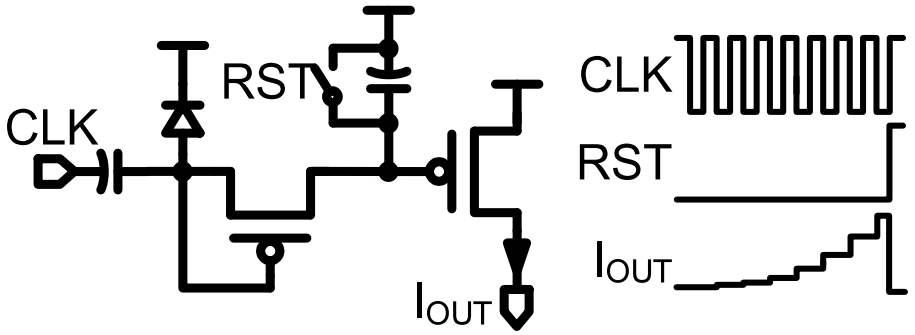
$$\sum I_{OUT} = I_{NORM}$$



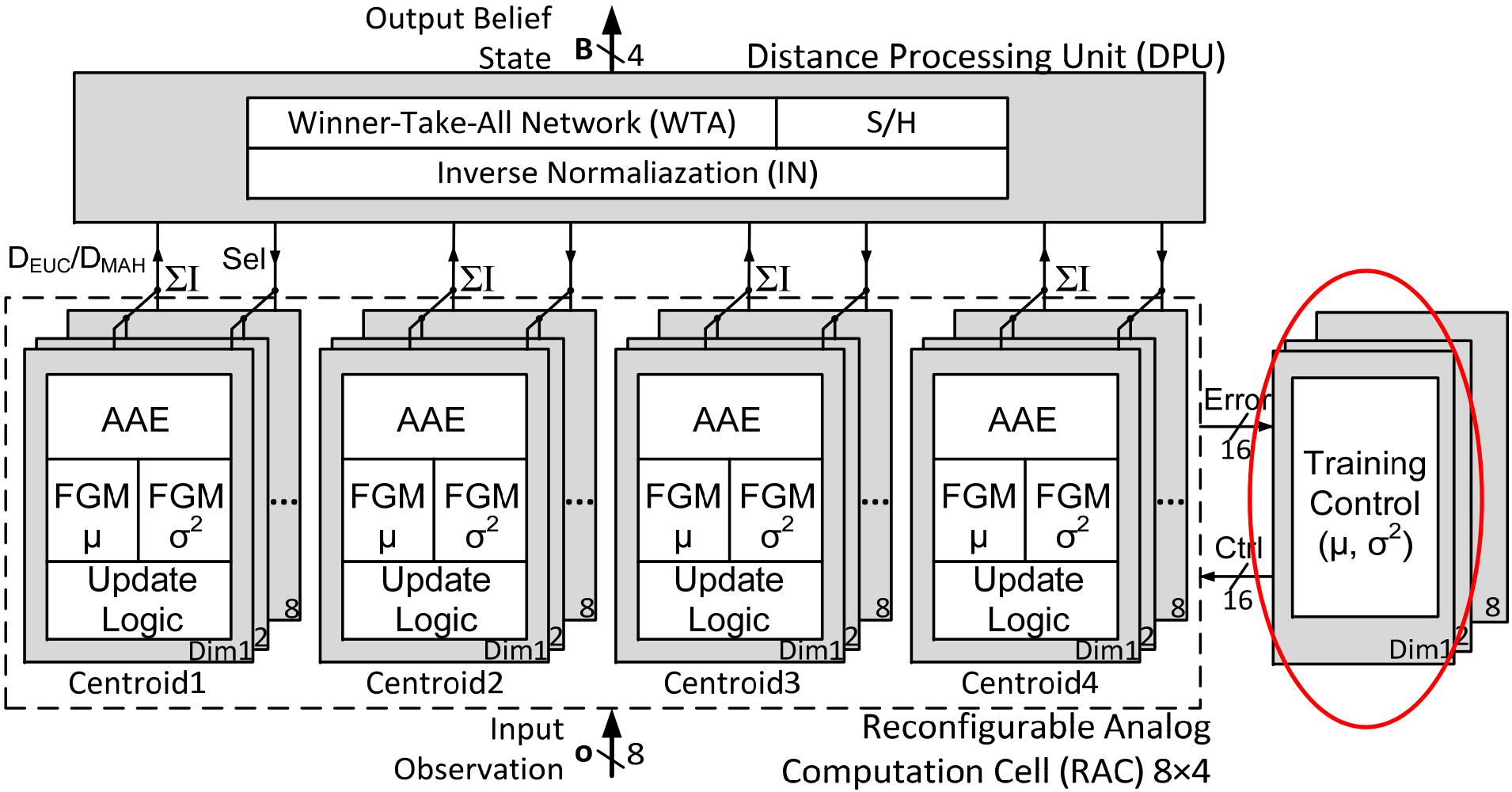
S/H and ST

- Holding capacitors realized with wiring parasitic
  - Low injection switch turned-on with reduced V_{GS}
- Centroids initialized too far away from populated regions suffer from starvation
  - ST injects additional current to force their occasional selection





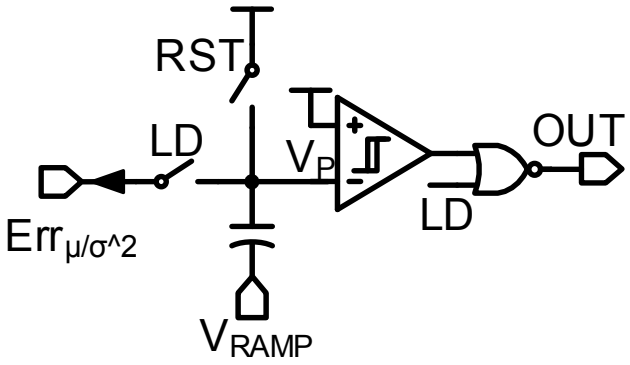
Training Control

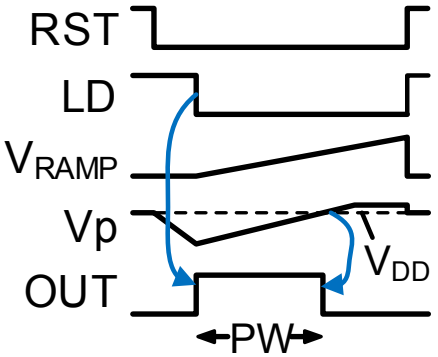


- AAE: analog arithmetic elements
- FGM: floating gate memory

Training Control

- Training pulse width proportional to the memory error current





- Memories converge to the input data statistics with proportional updates

$$PW_{\mu} = K \cdot Err_{\mu} = K(o - \hat{\mu})$$

$$PW_{\sigma^2} = K \cdot Err_{\sigma^2} = K\left(C^{-1}(o - \hat{\mu})^2 - \hat{\sigma}^2\right)$$

$$\hat{\mu}(n+1) = \hat{\mu}(n) + \alpha \cdot Err_{\mu}$$

$$\hat{\sigma}^2(n+1) = \hat{\sigma}^2(n) + \beta \cdot Err_{\sigma^2}$$

$$\hat{\mu} \rightarrow \mu(o)$$

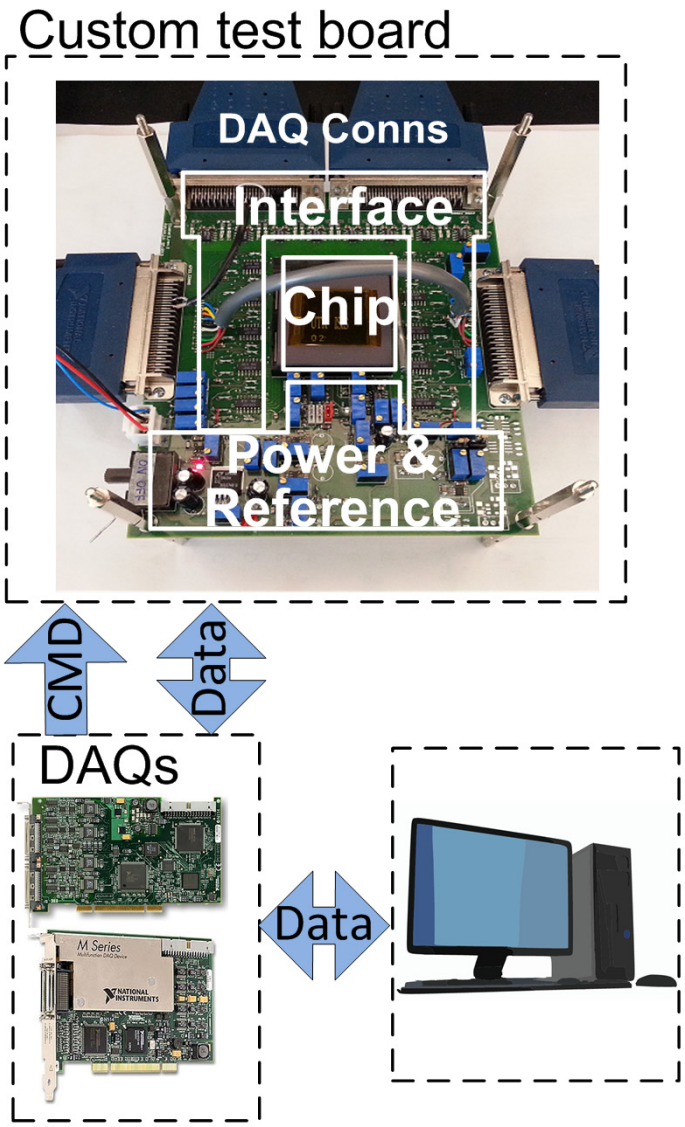
$$\hat{\sigma}^2 \rightarrow C^{-1} \cdot \sigma^2(o)$$

Outline

- Background and motivation
- Architecture and algorithm
- Circuit design
- Measurement results
  - Test Setup
  - Input Referred noise
  - Clustering
  - Pattern Recognition
- Conclusion

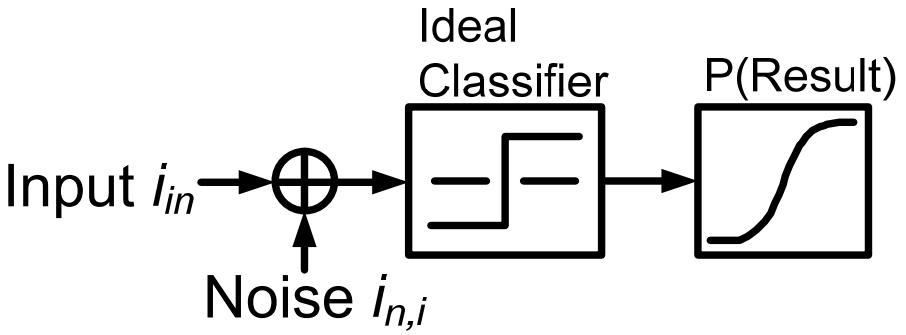
Test Setup

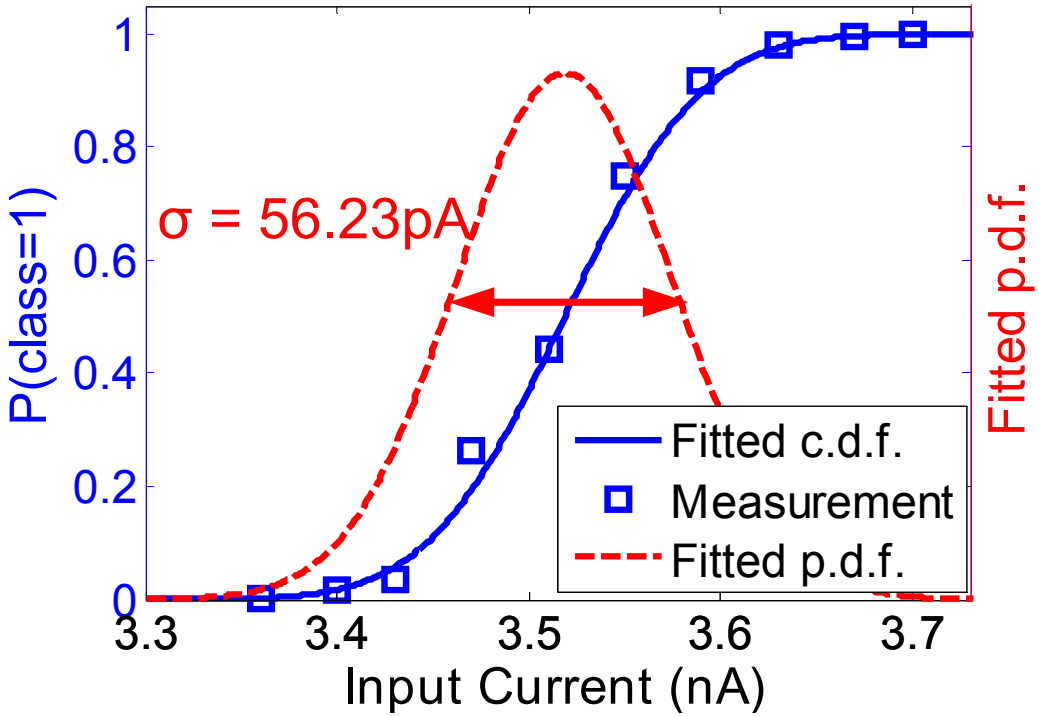
- Custom test board
  - Interfaces current mode IOs
- Data acquisition cards connected to host PC
  - Data conversion /streaming and operation command



System Input Referred Noise

- Noise causes classification uncertainty
- σ is extracted using curve fitting.
- $i_{n,i}$ = 56.23 pA_{rms}, i_{FS} = 10 nA
- SNR = 45 dB





Clustering Test

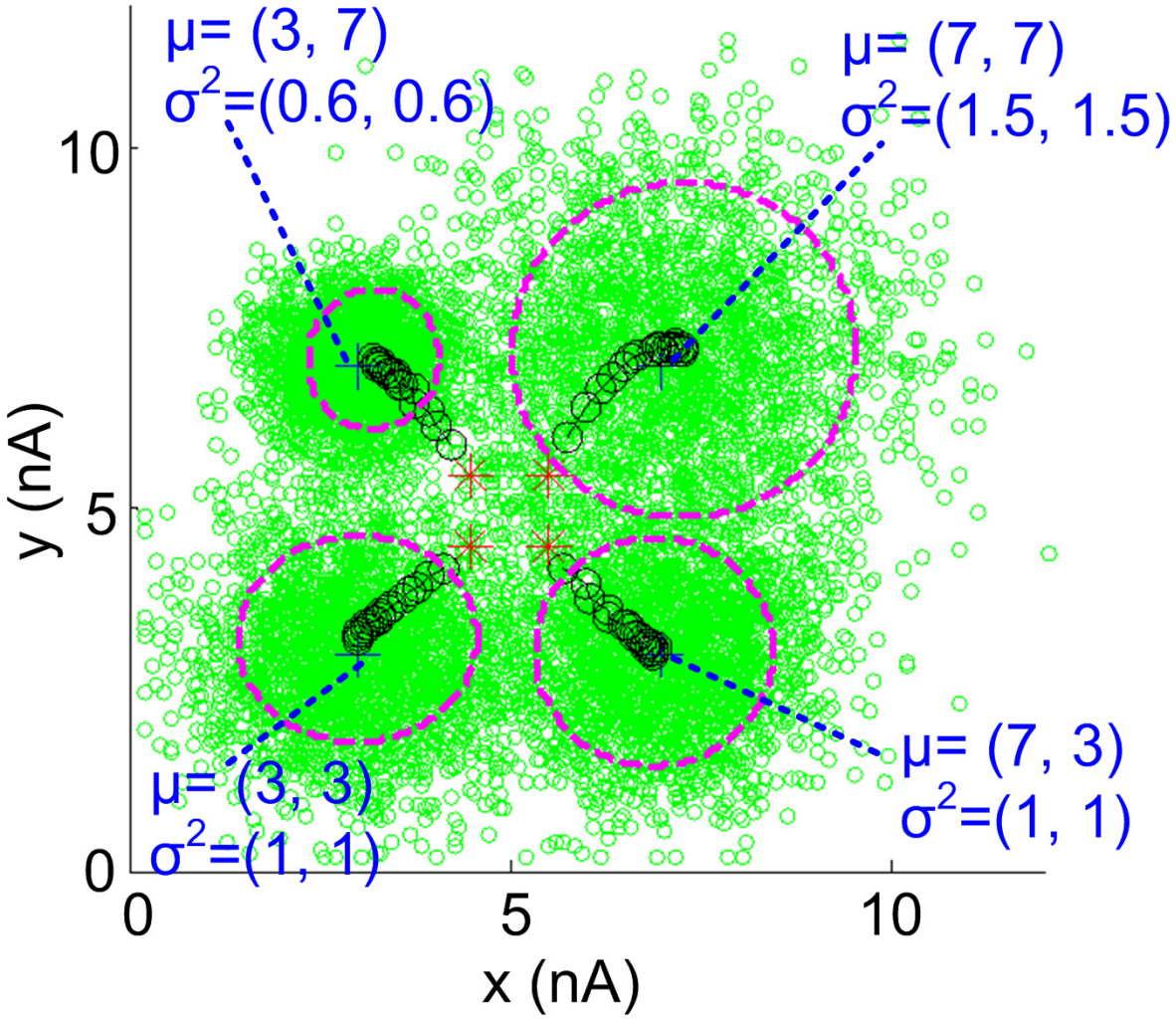
Input Data

Cluster Means

Evolution of Centroid Means

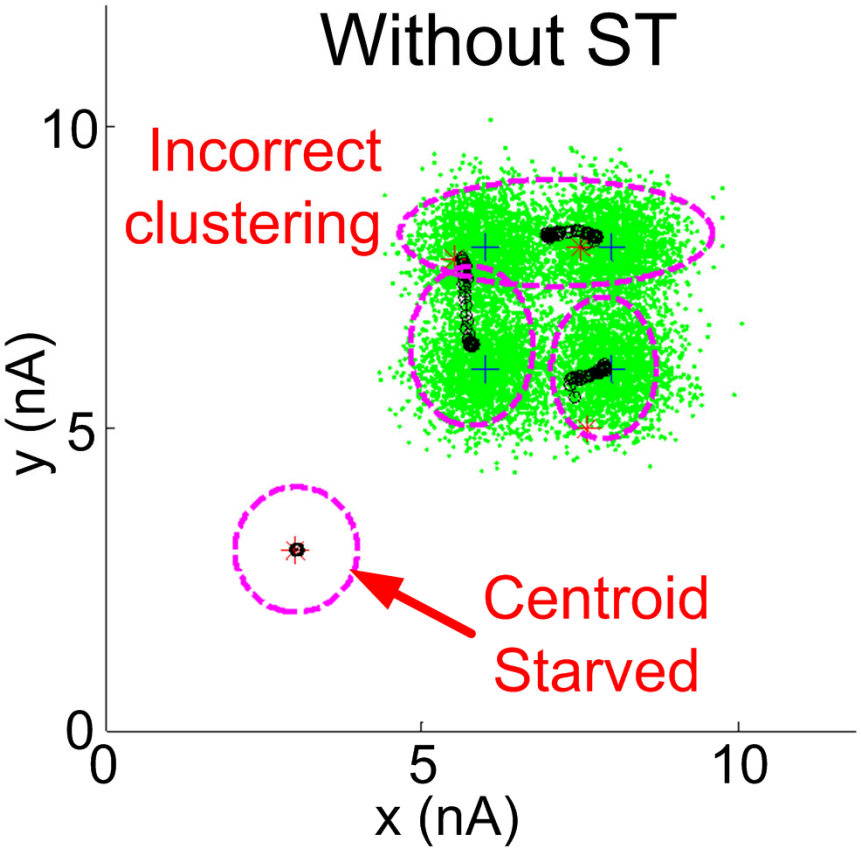
Extracted Variance

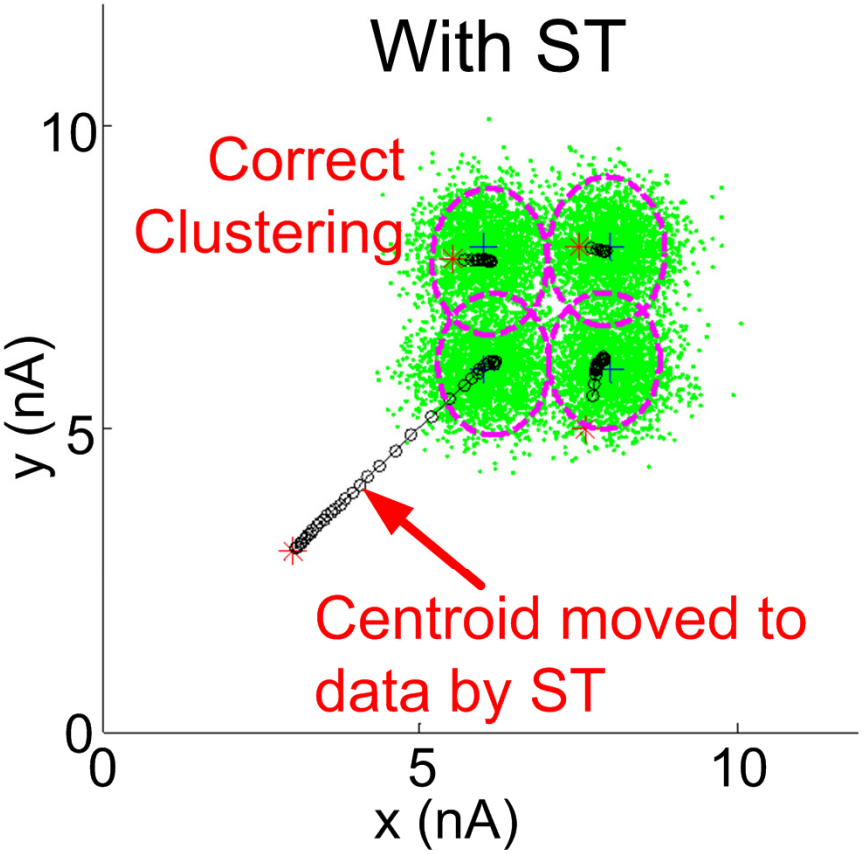
μ= Data Cluster
σ^2= Parameters



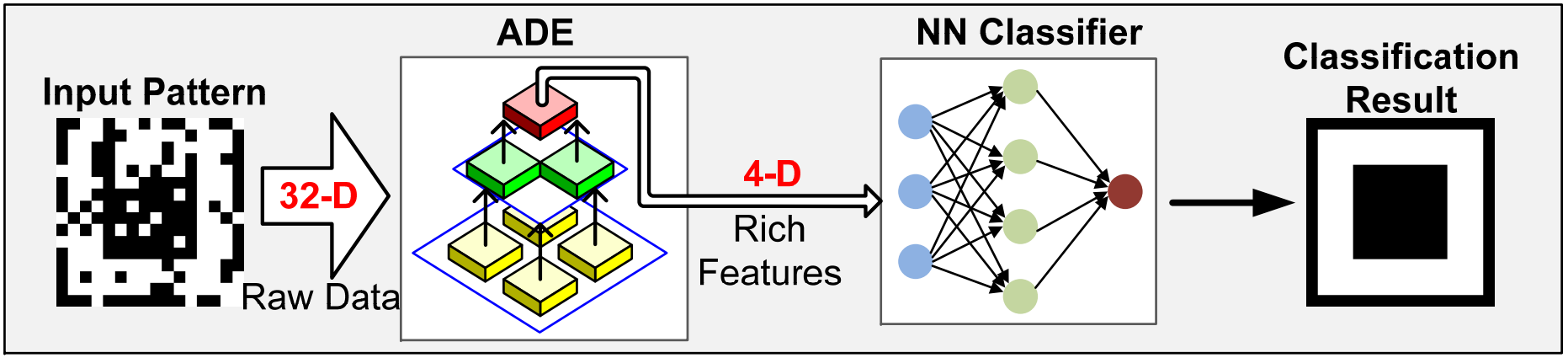
Clustering Test – Starvation Trace

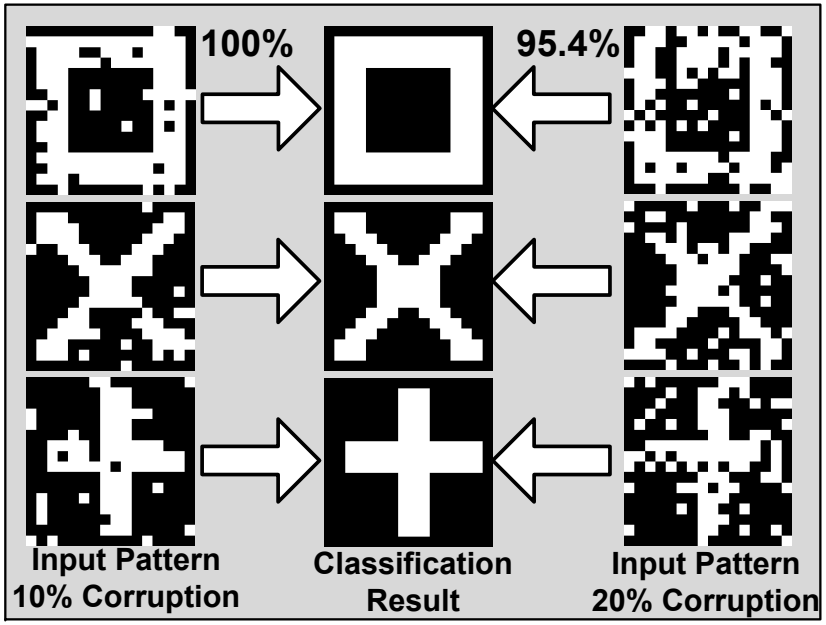
- Clustering test with unfavorable initial condition

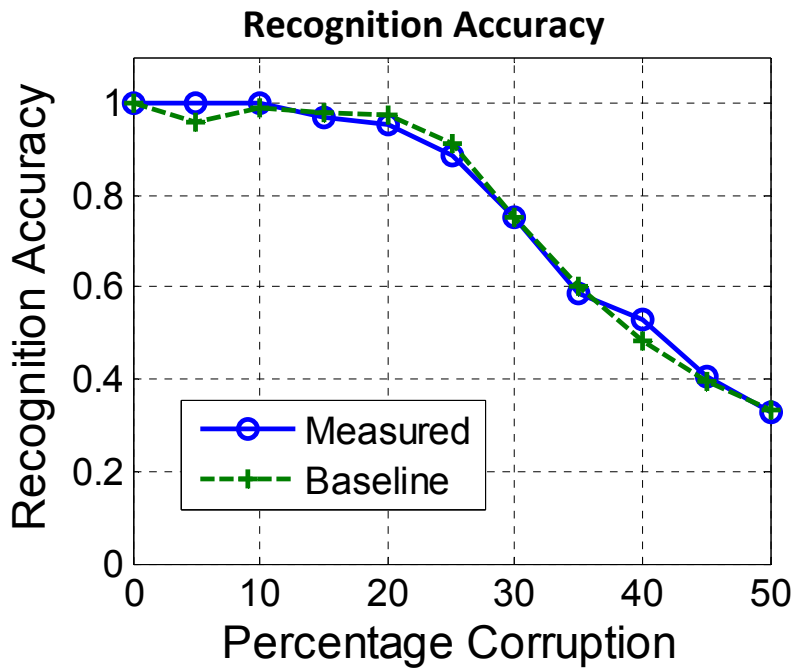




Pattern Recognition



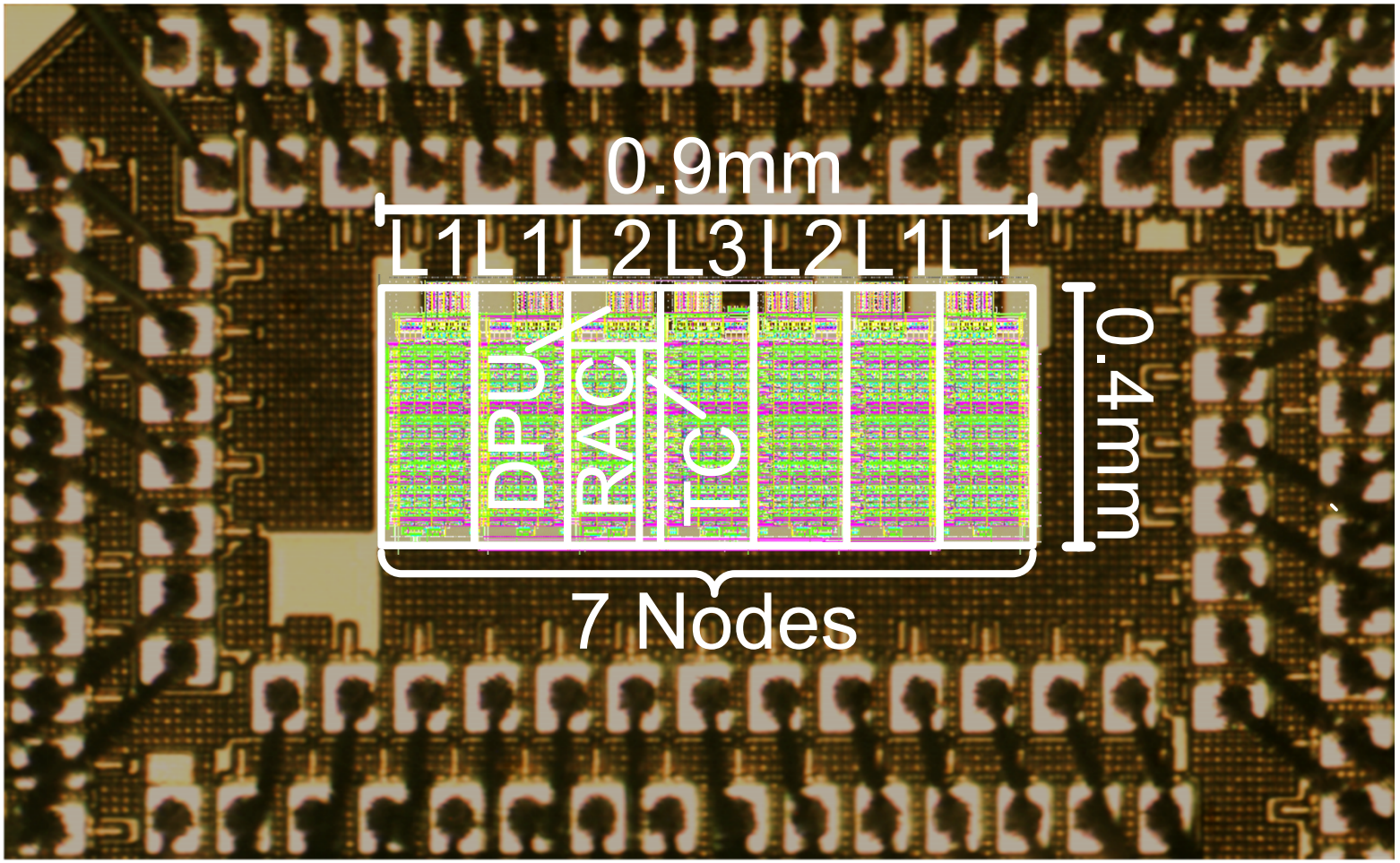




Performance Summary

Technology	1P8M 0.13μm CMOS	
Power Supply	3V (7V for tunneling)	
Active Area	0.9mm×0.4mm	
Memory SNR	46dB	
Input Noise	56.23pA$_{rms}$	
System SNR	45dB	
I/O Type	Analog Current	
Frequency	Training	4.5kHz
	Recognition	8.3kHz
Power	Training	27μW
	Recognition	11.4μW
Energy Efficiency	Training	480GOPS/W
	Recognition	1.04TOPS/W

Chip Micrograph



Conclusions

- An analog deep machine-learning engine featuring unsupervised online trainability and non-volatile memory is presented
- Demonstrates feature extraction with 8-fold dimension reduction and accuracy comparable to a floating-point software simulation
- Achieves very high energy efficiency in both modes, and peak energy efficiency of 1TOPS/W
- General purpose feature extraction engine ideal for autonomous sensory applications or as building block for large-scale learning systems